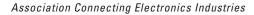
# IPC-A-600H-2010 **Acceptability of Printed Boards** April 2010 Supersedes IPC-A-600G July 2004 A standard developed by IPC





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### IPC-A-600H-2010

# Acceptability of Printed Boards

Developed by the IPC-A-600 Task Group (7-31a) of the Product Assurance Committee (7-30) of IPC

### Supersedes:

IPC-A-600G - July 2004 IPC-A-600F - November 1999 Users of this publication are encouraged to participate in the development of future revisions.

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### **Acknowledgment**

Any standard involving a complex technology draws material from a vast number of sources. While the principal members of the A-600 Task Group (7-31a) of the Product Assurance Committee (7-30) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of IPC extend their gratitude. Special thanks goes to the members of the Rigid Printed Board Committee (D-30) for their efforts in establishing acceptance criteria for printed boards.

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### Introduction

#### 1.1 SCOPE

This document describes the preferred, acceptable, and non-conforming conditions that are either externally or internally observable on printed boards. It represents the visual interpretation of minimum requirements set forth in various printed board specifications, e.g.; IPC-6010 series, J-STD-003, etc.

#### 1.2 PURPOSE

The visual illustrations in this document portray specific criteria of the requirements of current IPC specifications. In order to properly apply and use the content of this document, the printed board should comply with the design requirements of the applicable IPC-2220 series document and the performance requirements of the applicable IPC-6010 series document. In the event the printed board does not comply with these or equivalent requirements, then the acceptance criteria should be as agreed between user and supplier (AABUS).

#### 1.3 APPROACH TO THIS DOCUMENT

Characteristics are divided into two general groups:

- Externally Observable (section 2)
- Internally Observable (section 3)

"Externally observable" conditions are those features or imperfections which can be seen and evaluated on or from the exterior surface of the board. In some cases, such as voids or blisters, the actual condition is an internal phenomenon and is detectable from the exterior.

"Internally observable" conditions are those features or imperfections that require microsectioning of the specimen or other forms of conditioning for detection and evaluation. In some cases, these features may be visible from the exterior and require microsectioning in order to assess acceptability requirements.

Specimens should be illuminated during evaluation to the extent needed for effective examination. The illumination should be such that no shadow falls on the area of interest except those shadows caused by the specimen itself. It is recommended that polarization and/or dark field illumination be employed to prevent glare during the examination of highly reflective materials.

The illustrations in this document portray specific criteria relating to the heading and subheading of each page, with brief descriptions of the acceptable and nonconforming conditions for each product class. (See 1.4.) The visual quality acceptance criteria are intended to provide proper tools for the evaluation of visual anomalies. The illustrations and photographs in each situation are related to specific requirements.

The characteristics addressed are those that can be evaluated by visual observation and/or measurement of visually observable features.

Supported by appropriate user requirements, this document should provide effective visual criteria to quality assurance and manufacturing personnel.

This document cannot cover all of the reliability concerns encountered in the printed board industry; therefore, attributes not addressed in this issue **shall** be AABUS. The value of this document lies in its use as a baseline document that may be modified by expansions, exceptions, and variations which may be appropriate for specific applications.

When making accept and/or reject decisions, the awareness of documentation precedence must be maintained.

This document is a tool for observing how a product may deviate due to variation in processes. Refer to IPC-9191.

IPC-A-600 provides a useful tool for understanding and interpreting Automated Inspection Technology (AIT) results. AIT may be applicable to the evaluation of many of the dimensional characteristics illustrated in this document.

#### 1.4 CLASSIFICATION

This standard recognizes that electrical and electronic products are subject to classifications by intended end-item use. Three general end-product classes have been established to reflect differences in producibility, complexity, functional performance requirements, and verification (inspection/test) frequency. It should be recognized that there may be overlaps of product between classes.

Process Indicator imperfections are permitted and are deliverable.

The user is responsible for defining the product class. The procurement documentation package **shall** state the product class and any exceptions to specific parameters, where appropriate.

Criteria defined in this document reflect three classes, which are as follows:

**Class 1** — Includes limited life products suitable for applications where the requirement is function of the completed product.

**Class 2** — Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical.

**Class 3** — Includes products where continued high performance or performance-on-demand is critical, product downtime cannot be tolerated, and the product must function when required.

### **Introduction (cont.)**

Acceptability criteria in this document have been separated so that printed board product may be evaluated to any one of the three classes. The use of one class for a specific characteristic does not mean that all other characteristics must meet the same class. Selection should be based on minimum need. The customer has the ultimate responsibility for identifying the class to which the product is evaluated. Thus, accept and/or reject decisions must be based on applicable documentation such as contracts, procurement documentation, specifications, standards and reference documents.

#### 1.5 ACCEPTANCE CRITERIA

Most of the illustrations and photographs included in this document represent three levels of quality for each specific characteristic; i.e., Target Condition, Acceptable and Nonconforming. The text included with each level establishes the "Acceptance Criteria" for each class of product.

**Target Condition** in many cases is close to perfect. While this is the desired condition it is not always achievable and may not be necessary to ensure the reliability of the printed board in its service environment.

**Acceptable** indicates that the condition depicted, while not necessarily perfect, will maintain the integrity and reliability of the printed board in its service environment. The acceptable condition is considered acceptable for at least one or more classes but may not be acceptable for all classes, as specified by the associated acceptance criteria.

**Nonconforming** indicates that the condition depicted may be insufficient to ensure the reliability of the printed board in its service environment. The nonconforming condition is considered unacceptable for at least one or more classes of product but may be acceptable for other classes as specified by the associated acceptance criteria.

The target, acceptable and nonconforming conditions depicted herein and the associated acceptance criteria are intended to represent typical industrial practices. Requirements of individual product designs may deviate from these criteria.

The examples shown in the photographs and/or illustrations are sometimes exaggerated to make the referenced imperfection more apparent. The relationship between the text and the examples is not always parallel; it would be difficult to find many cases so specific that they would always match the acceptance criteria. When photographs or illustrations contained in this standard are not consistent with discussion in the written text, the written text takes precedence and should be followed.

It should also be noted that some of the photographs used may have more than one type of condition on the same example. It is necessary that the users of this document pay particular attention to the subject of each section to avoid misinterpretation.

It should be understood that the first inference to nonconformance given implies that all other conditions of lesser magnitude are acceptable. Thus, a criteria which states a nonconformance condition as 50% of the surface is pitted, for example, implies that anything less than 50% of the surface being pitted is acceptable for that characteristic in that class. Obviously, nonconformance in Class 1 implies nonconformance in Class 2 and Class 3; and likewise, nonconformance for Class 2 implies nonconformance in Class 3.

An inspector **shall not** make the selection as to which class the part under inspection belongs. When making accept and/or nonconformance decisions, the awareness of precedence of documentation must be maintained.

In all cases, documentation should be available to the inspector defining to which class the part submitted for inspection belongs.

Procedures and requirements for conducting visual inspections related to this document **shall** be in accordance with the requirements of the applicable performance specification.

In the event of conflict, the following order of precedence **shall** apply:

- Purchase Order (including exceptions to the master drawing, if any)
- Procurement documentation reflecting the customers detailed requirements (such as master drawing)
- 3. Other documents to the extent specified by the customer
- 4. The end item performance specification such as the IPC-6010 series when invoked by the customer
- This acceptability document. Printed boards should be of uniform quality and shall conform to the IPC-6010 series.

IPC-6010 series establishes the minimum acceptability requirements for printed boards. This document, IPC-A-600, is a companion and complementary document, providing pictorial interpretation of these requirements. It is not intended to be used as a performance specification for printed board manufacture or procurement.

IPC-A-600 can be used as a support document for inspection. It does not specify frequency of in-process inspection or frequency of end product inspection. Nor is the allowable number of nonconforming process indicators or the number of allowable repair/rework of defects specified.

Visual examination for applicable attributes **shall** be conducted at 3 diopters (approx.1.75X). If the acceptable condition of a suspected defect is not apparent, it should be verified at progressively higher magnifications (up to 40X) to confirm that it is a defect. Dimensional requirements such asspacing or conductor width measurements may require other

#### 1 INTRODUCTION

### **Introduction (cont.)**

magnifications and devices with reticles or scales in the instrument, which allow accurate measurements of the specified dimensions. Contract or specification may require other magnifications.

Plated-through holes (PTHs) **shall** be internally examined for foil and plating integrity at a magnification of 100X. Referee examinations **shall** be accomplished at a magnification of 200X.

Automated Inspection Technology (AIT) results may be applicable to the evaluation of many of the dimensional characteristics illustrated in this document.

**1.6 Applicable Documents** The following specifications of the revision in effect at the time of order form a part of this document to the extent specified herein. If a conflict of requirements exists between this specification and the listed applicable documents, this specification **shall** take precedence.

#### 1.6.1 IPC1

J-STD-003 Solderability Tests for Printed Boards

**IPC-T-50** Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-TM-650 Test Methods Manual<sup>2</sup>

2.1.1 Microsectionin	g
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<sup>2.1.1.2</sup> Microsectioning, Semi or Automatic Technique Microsection Equipment (Alternate)

IPC-SM-840 Qualification and Performance of Permanent Solder Mask

IPC-2220 Family of Design Documents

IPC-4562 Metal Foil for Printed Wiring Applications

**IPC-4781** Qualification and Performance Specification of Permanent, Semi-Permanent and Temporary Legend and/or Marking Inks

IPC-6010 Family of Board Performance Documents

**IPC-9191** General Requirements for Implementation of Statistical Process Control

**IPC-9691** User Guide for the IPC-TM-650, Method 2.6.25, Conductive Anodic Filament (CAF) Resistance Test (Electrochemical Migration Testing)

### 1.6.2 American Society of Mechanical Engineers<sup>3</sup>

**ASME B46.1** Surface Texture (Surface Roughness, Waviness and Lay)

#### 1.7 DIMENSIONS AND TOLERANCES

All dimensions and tolerances specified herein are applicable only to the end product. Dimensions are expressed in hard SI (metric) units and parenthetical soft imperial [inch] units.

Reference information is shown in parentheses ().

#### 1.8 TERMS AND DEFINITIONS

Terms and definitions **shall** be in accordance with IPC-T-50 and as defined in 1.8.1.

- **1.8.1 Process Indicator** A detectable anomaly, other than a defect, that is reflective of material, equipment, personnel, process and/or workmanship variation.
- **1.9 Revision Level Changes** Changes made to this revision of the IPC-A-600 are indicated throughout by grayshading of the relevant subsection(s). Changes to a figure or table are indicated by gray-shading of the figure or table header.

#### 1.10 WORKMANSHIP

Printed boards fabricated to the requirements of this document **shall** be processed in such a manner as to be uniform in quality and to preclude the introduction of dirt, foreign matter, oil, fingerprints, flux residues, or other contaminants that may affect the life or serviceability of the product. Printed boards **shall** be free of defects in excess of those allowed by this document. Acceptance of imperfections not specifically covered by this document *shall* be AABUS.

<sup>2.2.2</sup> Optical Dimensional Verification

<sup>2.3.25</sup> Detection and Measurement of Ionizable Surface Contaminants

<sup>2.4.1</sup> Adhesion, Tape Testing

<sup>2.4.22</sup> Bow and Twist

<sup>2.4.28.1</sup> Adhesion, Solder Resist (Mask), Tape Test Method

<sup>2.6.25</sup> Conductive Anodic Filament (CAF) Resistance Test (Electrochemical Migration Testing)

www.ipc.org

Current and revised IPC Test Methods are available on the IPC Web Site (www.ipc.org/html/testmethods.htm)

<sup>3.</sup> www.asme.org

#### 2 EXTERNALLY OBSERVABLE CHARACTERISTICS

### Introduction

This section addresses those characteristics which are observable from the surface. This includes those characteristics that are external and internal in the printed board but visible from the surface as follows:

- Surface Imperfections such as burrs, nicks, scratches, gouges, cut fibers, weave exposure and voids.
- Subsurface Imperfections such as foreign inclusions, measling/crazing, delamination, pink ring and laminate voids.
- Imperfections in Conductive Pattern such as loss of adhesion, reduction of conductor width or thickness due to nicks, pinholes, scratches, surface plating or coating defects.
- Hole Characteristics such as diameter, misregistration, foreign material, plating or coating defects and scratches.
- Marking Anomalies including location, size, readability, and accuracy.
- Solder Mask Surface Coating Imperfections such as misregistration, blisters, bubbles, delamination, adhesion, physical damage and thickness.
- **Dimensional Characteristics** including printed board size and thickness, hole size and pattern accuracy, conductor width and spacing, registration and annular ring.

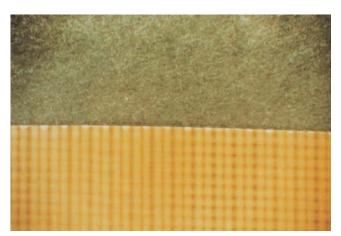
### 2.1 Printed Board Edges

Imperfections such as burrs, nicks or haloing along the edge of the printed board are acceptable provided they do not exceed the limits below.

### 2.1.1 Burrs

Burrs are characterized by small lumps or masses with an irregular shape, convex to a surface, and are a result of a machine process, such as drilling or gouging.

### 2.1.1.1 Nonmetallic Burrs



Target Condition - Class 1, 2, 3

• Edge conditions - smooth, no burrs.

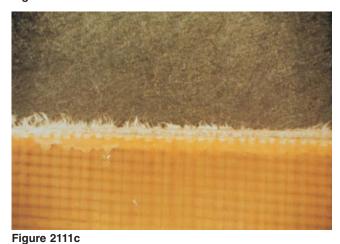
Figure 2111a



Acceptable - Class 1, 2, 3

- Edge conditions rough but not frayed.
- Edge conditions loose burrs do not affect fit and function.

Figure 2111b



### Nonconforming - Class 1, 2, 3

### 2.1 BOARD EDGES

### 2.1.1.2 Metallic Burrs

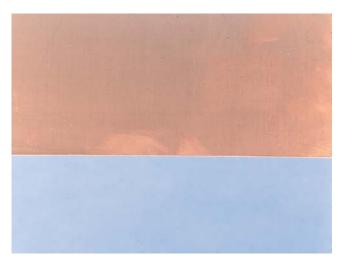


Figure 2112a



Figure 2112b

### Target Condition/Acceptable - Class 1, 2, 3

• Edges **shall** be clean cut and without metallic burrs.

### Nonconforming - Class 1, 2, 3

### **2.1.2 Nicks**



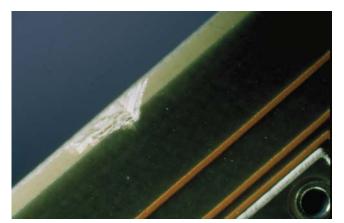


Figure 212b



Figure 212c

### Target Condition - Class 1, 2, 3

• Edge condition -smooth, no nicks.

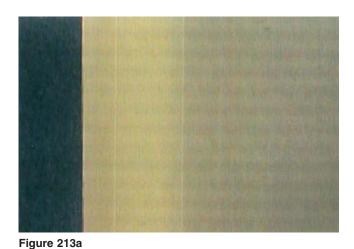
### Acceptable - Class 1, 2, 3

- Edges are rough but not frayed.
- Nicks do not exceed 50% of the distance from the printed board edge to the nearest conductor or 2.5 mm [0.0984 in], whichever is less.

### Nonconforming - Class 1, 2, 3

### 2.1 BOARD EDGES

### 2.1.3 Haloing



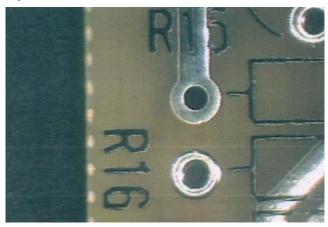


Figure 213b

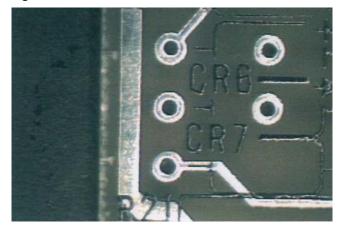


Figure 213c

### Target Condition - Class 1, 2, 3

• No haloing.

### Acceptable - Class 1, 2, 3

 Distance between the haloing penetration and the nearest conductive feature is not less than the minimum lateral conductor spacing, or 100 µm [3,937 µin] if not specified.

### Nonconforming - Class 1, 2, 3

### Introduction

### **Identification of Imperfections**

Nondestructive visual criteria have been established to aid in the identification and disposition of laminate defects. Refer to the following sections where definitions, illustrations and photographs have been provided which precisely define and identify the following conditions:

### Surface 2.2

• weave exposure	2.2.1
• weave texture	2.2.2
• exposed/disrupted fibers	2.2.3
• pits and voids	2.2.4

#### Subsurface 2.3

• measling	2.3.1
• crazing	2.3.2
• delamination/blister	2.3.3
• foreign inclusions	2.3.4

It is important to note that laminate defect conditions may exist when the fabricator receives the material from the laminator, or may become apparent during the fabrication of the printed board. Some defects may be induced during processing.

### 2.2.1 Weave Exposure

**Weave Exposure:** A surface condition of base material in which the unbroken fibers of woven cloth are not completely covered by resin.

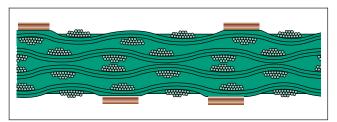


Figure 221a

Note: This graphic is for illustrative purposes only and does not require a microsection evaluation.

### Acceptable - Class 3

No weave exposure.

### Acceptable - Class 1, 2

• Excluding the area(s) with weave exposure, the remaining space between conductors meets the minimum conductor spacing requirement.

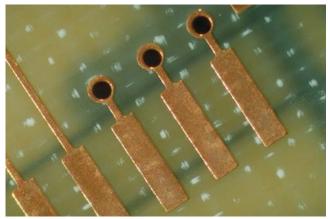


Figure 221b

### Nonconforming - Class 1, 2, 3

### 2.2.2 Weave Texture

**Weave Texture:** A surface condition of base material in which a weave pattern of cloth is apparent although the unbroken fibers of woven cloth are completely covered with resin.

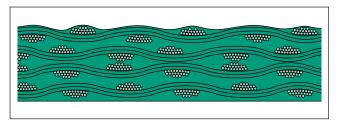


Figure 222a

Note: This graphic is for illustrative purposes only and does not require a microsection evaluation.

### Acceptable - Class 1, 2, 3

 Weave texture is an acceptable condition in all classes but is sometimes confused with weave exposure because of similar appearances.

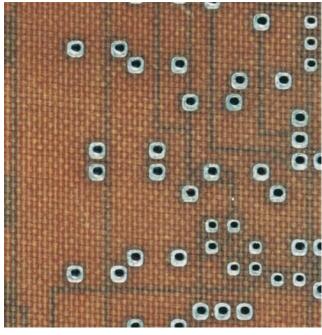


Figure 222b

Figure 222b is an example of a surface condition that could be either weave exposure or weave texture. The difference cannot be determined from this view. The difference can be discerned using nondestructive tests (oblique illumination with microscope) or micro-section.

### 2.2.3 Exposed/Disrupted Fibers

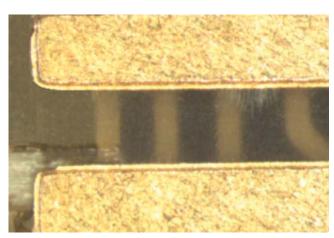


Figure 223a

### Acceptable - Class 1, 2, 3

• Exposed or disrupted fibers do not bridge conductors and do not reduce the conductor spacing below the minimum requirements.

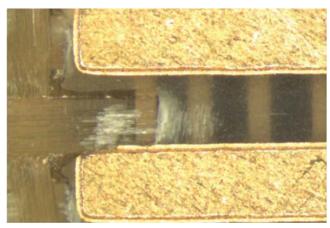
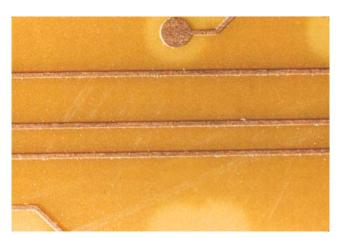


Figure 223b

### Nonconforming - Class 1, 2, 3

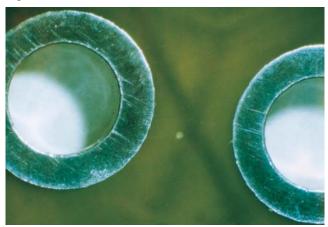
### 2.2.4 Pits and Voids



Target Condition - Class 1, 2, 3

• No pits or voids.

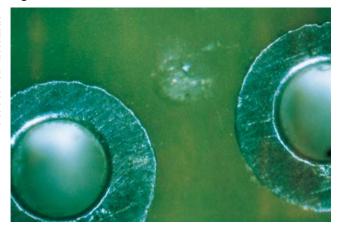
Figure 224a



Acceptable - Class 1, 2, 3

- Pits or voids do not exceed 0.8 mm [0.031 in].
- Total printed board area affected is less than 5% per either side.
- Pits or voids do not bridge conductors.

Figure 224b



Nonconforming - Class 1, 2, 3

Figure 224c

### Introduction

This section is focused on those subsurface conditions of laminated base materials that are externally observable through the base material itself and some solder mask coatings. The most frequent subsurface base material conditions are termed measling, crazing, delamination, blistering and foreign materials. These conditions may be observed throughout the printed board manufacturing and inspection process; such as:

- During incoming metal-clad base material evaluations after being manufactured by the laminator,
- By the printed board manufacturer after having removed (etched) the metal cladding in the preparation of "inner-layer" details for multilayer printed boards,
- After etching the "outer" layers of printed board to form the required arrangement of conductive patterns and markings,
- After baking operations (such as solder mask or component legends),
- After thermal shock, as in solder fusing/coating or solderability testing processes.

Base material subsurface conditions have been the subject of considerable discussion within the printed board industry for several decades. Of the several subsurface conditions, measling and crazing continue to cause the most concerns. Measles and crazing have been the primary focus of three IPC "Blue Ribbon Committees" of experts. The following are brief summaries and additional comments from the IPC Blue Ribbon Committees:

### Brief summary of the First IPC Blue Ribbon Committee on Measles

This first committee conducted a wide overview of printed board base material surface and subsurface conditions with a major focus on measles. IPC's "Measles in Printed Wiring Boards, Information Document" was published in 1973 as a result of this effort. The committee was to collect as much data as was available on measles and other surface/ subsurface conditions; and to standardize the terms, definitions (descriptions), photographs, and illustrations of surface and subsurface conditions. It was felt that sufficient research had been done by industry and that a position on "measles" could be prepared by the committee. The committee's recommendation was as follows, "comprehensive review of available literature and available research and test data, that while measles may be objectionable cosmetically, their effect on functional characteristics of finished products, are at worst minimal, and in most cases insignificant."

Comments: Despite the committee's recommendation and industry data, there was still a strong reluctance by most government and industry personnel to accept that measles are a cosmetic condition with no functional effect in most applications. Most companies continued to retain "no measling" requirements in their specifications. But when measles or

other nonconforming surface/subsurface conditions had severe impact on their production schedules, the customer (or acceptance agency) would produce a document that established acceptance guidelines for measles (and frequently other surface and subsurface conditions). The new guidelines were based on size, percent reduction in conductor spacing, and amount of affected area. They also varied from customer-to-customer. As technology evolved, in particular reductions in conductor spacing, the effect of measling and other surface/subsurface conditions once again became a serious industry wide concern. As a result, a second IPC Blue Ribbon Committee on Measles was formed.

### Brief summary of the Second IPC Blue Ribbon Committee on Measles

This second committee was formed in late 1978. This committee reviewed the findings of the first committee, solicited the industry for additional data, and reviewed the proprietary acceptance criteria provided by IPC members. The Second Blue Ribbon Committee came to the same conclusion. Measles are a cosmetic process indicator and had almost no reported effects on a product's functional performance in most applications. The major exception was high voltage applications. There was still reluctance by some government organizations and a few industrial companies to categorically accept measles. As such, this committee established a set of measling/crazing requirements that obtained consensus from all IPC members. The result was a matrix of acceptance limitations for the three major phases of the printed board electronic assembly process: laminated material, printed board final inspection, and after printed board assembly. These requirements included percent reductions in conductor spacing (not exceeding minimum conductor spacing), and various amounts of measled area for each side of the printed board (or assembly) based on the Class of product. These requirements were added as an amendment to the first printing of the IPC-A-600, Revision C, and were included in later printings of the C revision and, in a different format, the IPC-A-600, Revision D.

Comments: The primary concerns expressed by the reluctant individuals are summarized in the following list (with comments):

- Electrical Insulation Resistance, both volume and surface several reports and available test data indicates that insulation resistance is not significantly affected by measling or crazing.
- Contamination the concern was that ionic materials could diffuse or be "pumped" (by alternating atmospheric pressure) into measles or crazing and would result in lower insulation resistance or conductive anodic filament (CAF) growths, shorts. Salt spray tests indicated this was not a valid premise, and most ionic materials (such as salts) will not diffuse into the base material.

### **Introduction (cont.)**

- Applied Voltages high voltage applications are a concern (in particular where there is the possibility of "corona" in the measling or crazing) the dielectric strength is reduced by 20-50% in comparison to a similar non-measled/crazed area, in particular at altitudes greater than 20 km [12.43 miles].
- Environmental most measling/crazing did not appear to increase in size or occurrence due to environmental testing.

IPC-A-600, Revision E, was the first revision to reflect the needs for surface mounted component technology. As such, the acceptance requirements for measling and crazing were separated. For measles, the acceptance requirements allowed bridging under surface conductor spacing. This was done based on the definition of measles, test data, and industry experience of measles having never been documented to cause a functional failure. Crazing is much less controlled separation in the base material forming "interconnections" between measles and possibly adjacent conductive patterns; therefore, the acceptance requirements for crazing were set the same as the similar conditions of delamination and blistering.

Over a period of time, governing specifications have become excessively heavy regarding the presence of measles. In addition, cosmetic appearance has become a major acceptance criterion. In actual fact, no failure has ever been attributed to measling, based on all military and industry testing to date. IPC, industry and various military agencies have conducted extensive testing in severely measled assemblies under extreme environmental conditions for long periods of time with no evidence of growth, spreading or any detriment to the function of the assembly. Measles should not be the cause for rejection.

Measling is an internal condition occurring in the woven fiber reinforced laminated base material in which the bundles are separated at the weave intersection. The term "crazing" is sometimes used to describe an array of measles which appear from the surface to be interconnected. When the measles look to be interconnected, this condition called "crazing" is a form of delamination in that there are separations along the length of the fiber/yarns and the resin. For non-woven material, this condition resembles a measle but is randomly located and has an irregular shape (see Figure 23a).

In a case study done, the prime cause of the observed measles was a combination of moisture, which diffuses readily into epoxy-glass, and component soldering temperatures. The application of local high temperatures for component mounting caused entrapped moisture to vaporize and break the epoxy-glass bond at the "knuckle" (intersection of the warp and fill of the e-glass cloth). From previous experience, it

is known that epoxy-glass absorbs atmospheric moisture, and when moisture content exceeds 0.3 wt%, it can give rise to measling during solder dip/level and/or assembly soldering operations.

There are other factors that can contribute to measles/crazing such as: resin composition, method of making laminates, coupling agents,  $T_{\rm g}$ , etc. In the past, reports were compiled which revealed that measles and crazing with over 50% spacing violation were not adverse to the reliability of the hardware. Why, if all test reports showed no problems with measles and no reported field failures, are we so concerned about measles and crazing? Because it appears feasible, in theory, that if measles with 100% conductor spacing violation combines with moisture or some other contaminant, copper migration (IR failures) should be experienced between conductors.

Even when the potential failure mechanism mentioned above is analyzed, it is almost impossible to experience such (IR/migration) failure. First, a measle(s) gapping conductive patterns is needed. Secondly, moisture in the printed board/assembly, along with a conductive or ionic contaminant such as chlorides, is necessary.

In this instance, a typical industry example, the measle is at the center between two plated through holes (see Figure 23b). The measle is 0.4 mm [0.0157 in] wide. In order to get possible copper migration, the measle had to gap the two plated through holes. This of course would be most unlikely. The second example (see Figure 23c) illustrates what is required for a potential failure mechanism between two surface conductors. A (+) conductor directly over a knuckle is required and a (-) conductor is also required directly over a knuckle. For an electrical short to occur between these conductors through the base material, there would need to be a conductive path from one conductive pattern, through the remaining dielectric materials (resin and yarn) to the separation (measle), along the separation in the direction of the other conductive pattern, once again through the remaining dielectric materials (resin and yarn), and to the second conductive pattern. In order to induce a failure all of the above mentioned ingredients are required along with a voltage potential between two adjacent conductors. This occurrence is highly unlikely and is most likely why the industry has not experienced any adverse reliability problems due to measles.

When making acceptance calls on electronic hardware, consider all the possible concerns mentioned above. Measles should not be considered a nonconforming condition. It should instead be considered a process indicator, telling you that the process is on the verge of going out of control. Correct the problem, but do not scrap the product, taking into account all of the above mentioned variables.

### **Introduction (cont.)**

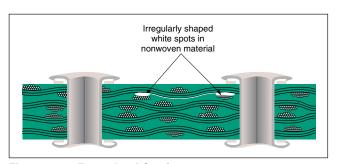


Figure 23a Example of Crazing

Note: This graphic is for illustrative purposes only and does not require a microsection evaluation.

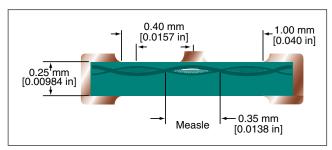


Figure 23b Example of Measle Gapping Conductive Patterns

Note: This graphic is for illustrative purposes only and does not require a microsection evaluation.

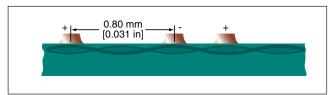


Figure 23c Example of Potential Failure Mechanism Between Two Surface Conductors

Note: This graphic is for illustrative purposes only and does not require a microsection evaluation.

### Brief summary of the Third IPC Blue Ribbon Committee on Measles

In 2004, the issue of printed board laminate degradation caused by internal Conductive Anodic Filament (CAF) growth came to the forefront of discussions among the IPC printed board assembly standards groups (including the 7-31b IPC-A-610 and 5-22a National Standard for Soldering task groups.) It was observed that circuit density, operating speed, band pass and reduced operating voltage had impacted the ability of circuits to operate under conditions supporting dendrite or CAF development.

With the proliferation of finer line conductors and reduced spacing in current designs, discussions within the assembly standards groups questioned the role of measles within printed board laminate materials as a potential catalyst for CAF growth.

For years, IPC standards for electronic production contained no restrictions for the occurrence of measles in printed boards and/or assemblies. Theoretically, measles could be continuous between conductors and could exist throughout the printed board. It was noted that this allowance was based on studies conducted nearly 30 years earlier based on circuit designs from that time period. It was recognized that a need existed to reconsider the measles requirements for today's production designs and product environment.

In the interim, as a means to call attention to this potential problem, IPC assembly documents were changed to include pass/fail (defect) criteria for Class 3 assemblies that exhibited the visual appearance of measles.

The new measles criteria created in the assembly documents defined requirements that were stricter than those given in the printed board documents unless the additional IPC-6012, Class 3A (Military and Aerospace) requirements were considered. IPC-6012, Class 3A does not allow measles in bare boards for these industry segments, however Class 3 printed boards produced in accordance with 6012, which exhibited measles, were no longer acceptable for use in the assembly documents for Class 3 in general. This requirement conflict was brought to the attention of the IPC Technical Activities Executive Committee (TAEC) and that body directed both groups to work together to come to some resolution, based on test data that would bring the documents into agreement on the acceptance criteria.

The leadership of the printed board standards committees formed a new Blue Ribbon Committee on Measles and designed and performed testing to determine if measles contributed to CAF failures in actual end product. This test protocol was completed in late 2006 and presented to the printed board standards committees at IPC Printed Circuits Expo/APEX 2007. There was conclusive evidence within the test that measles did not contribute to CAF growth; nor did the presence of measles promote CAF failures in the end product that exhibited CAF.

This presentation was then given to the assembly standards groups for their consideration. The request was made that the requirements in the bare printed board and assembly documents be changed to track with each other.

The leadership of the assembly standards groups concurred that the industry now had test data that addressed their original concerns regarding the potential of measles to promote CAF failures. They also agreed that the documents should be amended to eliminate the conflicting measles requirements. The groups jointly drafted the words, comments, and instructions for all documents regarding measles and these were presented to the committee membership at the 2007 IPC Midwest Conference. Copies of the test protocol summary are available through the IPC.

### 2.3.1 Measling

**Measling:** Measling manifests itself in the form of discrete white squares or "crosses" below the surface of the base material, and is usually related to thermally induced stress. Measles are subsurface phenomena that have been found in new laminated materials and in every board type made from woven fiber reinforced laminates at one time or another. Since measles are strictly subsurface phenomena and occur as a separation of fiber bundles at fiber bundle intersections, their apparent positions relative to surface conductors have no significance.

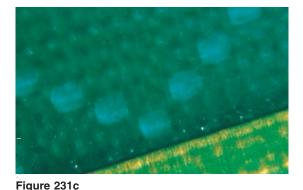


Measling

Figure 231b

Note: This graphic is for illustrative purposes only and does not require a microsection evaluation.

Figure 231a



#### Target - Class 1, 2, 3

No evidence of measling.

#### Acceptable - Class 1, 2

• The criteria for measling is that the printed board is functional.

### **Process Indicator - Class 3**

 Measled areas in laminate substrates exceed 50% of the physical spacing between noncommon conductors.

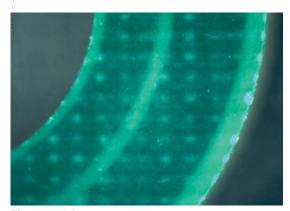


Figure 231d

**Note:** Measling is an internal condition which does not propagate as a result of thermal testing that replicates future assembly processes and has not been conclusively shown to be a catalyst for CAF growth. Delamination is an internal condition which may propagate under thermal stress and may be a catalyst for CAF growth. The IPC-9691 user's guide for CAF resistance testing and IPC-TM-650, Method 2.6.25, provide additional information for determining laminate performance regarding CAF growth. Users who wish to incorporate additional criteria for measle conditions may consider incorporating the provisions of IPC-6012, Class 3A which does not allow measles.

Note: Measles are observed from the surface. Cross-sections are for illustration purposes.

### 2.3.2 Crazing

**Crazing:** An internal condition occurring in the laminated base material in which the fibers within the yarn are separated. This can occur at the weave intersections or along the length of the yarn. This condition manifests itself in the form of connected white spots or "crosses" below the surface of the base material, and is usually related to mechanically induced stress. When the crosses are connected the condition is evaluated as follows:

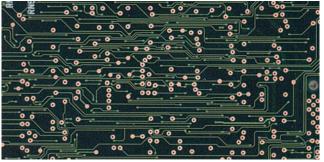


Crazing

Figure 232b

Note: This graphic is for illustrative purposes only and does not require a microsection evaluation.

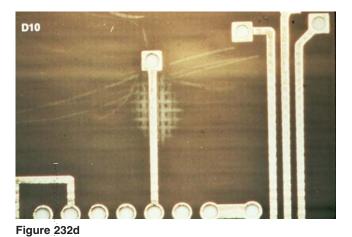
Figure 232a



Target Condition - Class 1, 2, 3

• No evidence of crazing.

Figure 232c



Acceptable - Class 2, 3

- The imperfection does not reduce the conductor spacing below the minimum.
- The distance of crazing does not span more than 50% of the distance between adjacent conductive patterns that are not electrically common.
- No propagation as a result of thermal testing that replicates the manufacturing process.
- Crazing at the edge of the printed board does not reduce the minimum distance between printed board edge and conductive pattern; or more than 2.5 mm [0.0984 in] if not specified.

Note: Crazing is observed from the surface. Cross-sections are for illustration purposes only.

### 2.3.2 Crazing (cont.)

### Acceptable - Class 1

- The imperfection does not reduce the conductor spacing below the minimum.
- No propagation as a result of thermal testing that replicates the manufacturing process.
- Crazing at the edge of the printed board does not reduce the minimum distance between printed board edge and conductive pattern; or more than 2.5 mm [0.0984 in] if not specified.

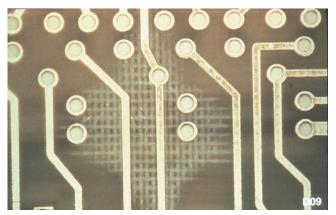


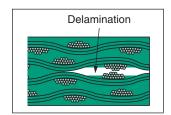
Figure 232e

### Nonconforming - Class 1, 2, 3

### 2.3.3 Delamination/Blister

**Delamination:** A separation between plies within a base material, between a material and conductive foil, or any other planar separations within a printed board.

**Blister:** Delamination in the form of a localized swelling and separation between any of the layers of a lamination base material, or between base material and conductive foil or protective coating.



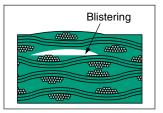


Figure 233a

Note: This graphic is for illustrative purposes only and does not require a microsection evaluation.

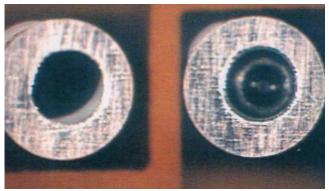


Figure 233b

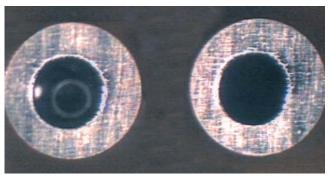


Figure 233c

#### Target Condition - Class 1, 2, 3

• No blistering or delamination.

#### Acceptable - Class 2, 3

- The area affected by imperfections does not exceed 1% of the printed board area on each side.
- The imperfection does not reduce the space between conductive patterns below the minimum conductor spacing.
- The blister or delamination does not span more than 25% of the distance between adjacent conductive patterns.
- No propagation as a result of thermal testing that replicates the manufacturing process.
- The imperfection does not exceed the specified minimum distance between printed board edge and conductive pattern, or 2.5 mm [0.0984 in] if not specified.

### 2.3.3 Delamination/Blister (cont.)

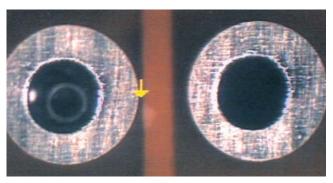


Figure 233d

### Acceptable - Class 1

- The area affected by imperfections does not exceed 1% of the printed board area on each side.
- The blister or delamination spans more than 25% of the distance between conductors, but does not reduce the space between conductor patterns below the minimum conductor spacing.
- No propagation as a result of thermal testing that replicates the manufacturing process.
- The imperfection does not exceed the specified minimum distance between printed board edge and conductive pattern, or 2.5 mm [0.0984 in] if not specified.

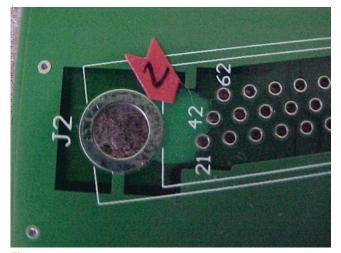


Figure 233e

### Nonconforming - Class 1, 2, 3

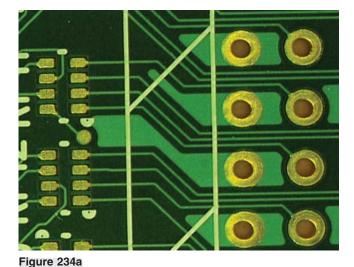
• Defects either do not meet or exceed above criteria.

**Note:** The area affected is determined by combining the area of each imperfection and dividing by the total area of the printed board. A separate determination is made for each side.

### 2.3.4 Foreign Inclusions

Foreign Particles: Metallic or nonmetallic, which may be entrapped or embedded in an insulating material.

Foreign material may be detected in raw laminate, B stage, or processed multilayer printed boards. The foreign objects may be conductive or nonconductive, and both types may be nonconforming depending on size and location.



### Target Condition - Class 1, 2, 3

• No foreign inclusions.

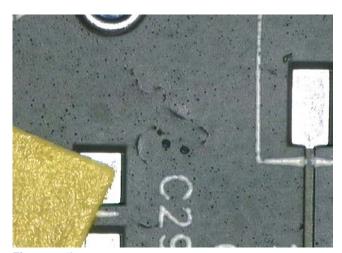


Figure 234b

### Acceptable - Class 1, 2, 3

- Translucent particles trapped within the printed board.
- Opaque particles trapped within the printed board which do not reduce the spacing between adjacent conductors to below the minimum spacing specified in the IPC-6010 series.
- Electrical parameters of the printed board are unaffected.

### 2.3.4 Foreign Inclusions (cont.)

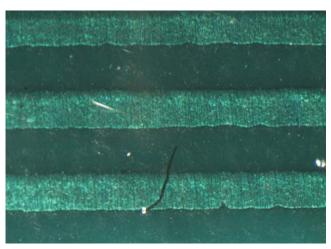


Figure 234c

### Nonconforming - Class 1, 2, 3

### 2.4.1 Nonwetting

Nonwetting: The inability of molten solder to form a metallic bond with the basis metal.

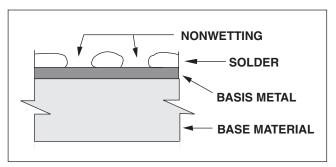


Figure 241a

Note: This graphic is for illustrative purposes only and does not require a microsection evaluation.

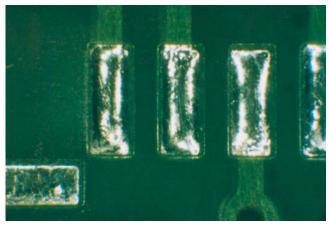


Figure 241b

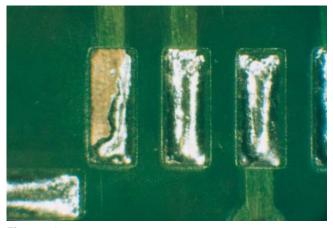


Figure 241c

### Target Condition - Class 1, 2, 3

• No nonwetting.

### Acceptable - Class 1, 2, 3

• Complete wetting on all conductive surfaces where solder is not excluded by mask or other plating finish. Vertical sides (conductor and land) areas may not be covered.

### Nonconforming - Class 1, 2, 3

### 2.4.2 Dewetting

**Dewetting:** A condition that results when molten solder coats a surface and then recedes to leave irregularly-shaped mounds of solder that are separated by areas that are covered with a thin film of solder and with the basis metal not exposed.

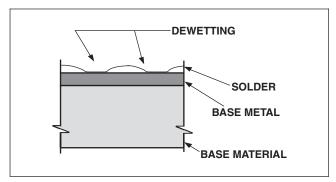


Figure 242a

Note: This graphic is for illustrative purposes only and does not require a microsection evaluation.



Figure 242b



Figure 242c

### Target Condition - Class 1, 2, 3

No dewetting.

### Acceptable - Class 2, 3

- On conductors and ground or voltage planes.
- On 5% or less of each land area for solder connection.

### Acceptable - Class 1

- On conductors and ground or voltage planes.
- On 15% or less of each land area for solder connection.

### 2.4 SOLDER COATINGS AND FUSED TIN LEAD

### 2.4.2 Dewetting (cont.)

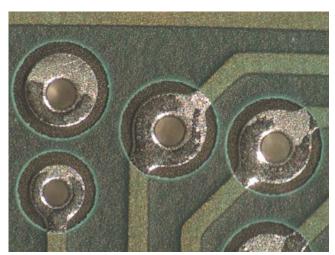
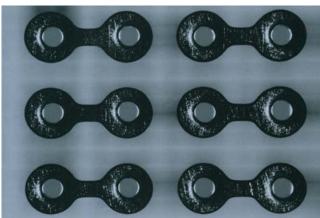


Figure 242d

### Nonconforming - Class 1, 2, 3

### 2.5.1 Nodules/Burrs



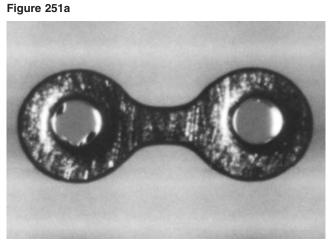


Figure 251b

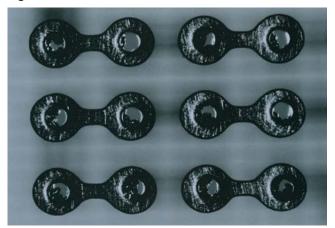


Figure 251c

### Target Condition - Class 1, 2, 3

• No evidence of nodules or burrs.

### Acceptable - Class 1, 2, 3

• Allowed if minimum finished hole diameter is met.

### Nonconforming - Class 1, 2, 3

### 2.5 HOLES - PLATED-THROUGH - GENERAL

### 2.5.2 Pink Ring

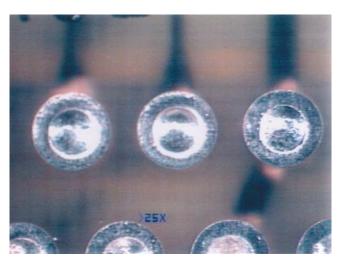


Figure 252a

### Acceptable - Class 1, 2, 3

No evidence exists that pink ring affects functionality. The
presence of pink ring may be considered a process indicator but is not nonconforming. The focus of concern should
be the quality of the lamination bond and hole cleaning and
conditioning processes.

### 2.5.3 Voids - Copper Plating

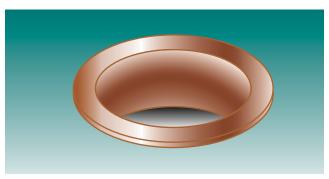


Figure 253a

### Target Condition - Class 1, 2, 3

No voids.

### Acceptable - Class 3

• No evidence of voids in the hole.

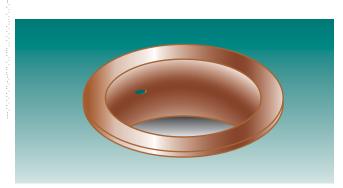


Figure 253b

### Acceptable - Class 2

- No more than one void in any hole.
- Not more than 5% of the holes have voids.
- Any void is not more than 5% of the hole length.
- The void is less than 90° of the circumference.

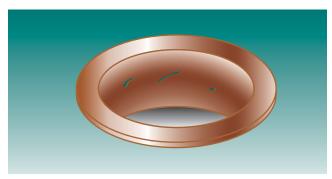


Figure 253c

### Acceptable - Class 1

- No more than three voids in any hole.
- Not more than 10% of the holes have voids.
- Any void is not more than 10% of the hole length.
- All voids are less than 90° of the circumference.

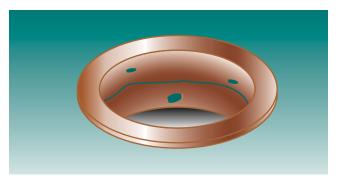
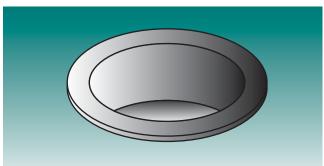


Figure 253d

### Nonconforming - Class 1, 2, 3

### 2.5.4 Voids - Finished Coating



No voids.

Target Condition - Class 1, 2, 3

Figure 254a

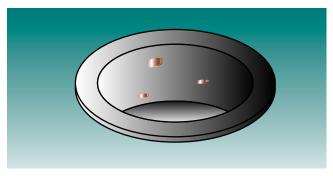


Figure 254b

### Acceptable - Class 3

- No more than one void in any hole.
- Not more than 5% of the holes have voids.
- The void is not more than 5% of the hole length.
- The void is less than 90° of the circumference.

### Acceptable - Class 2

- No more than three voids in any hole.
- Not more than 5% of the holes have voids.
- Any void is not more than 5% of the hole length.
- All voids are less than 90° of the circumference.

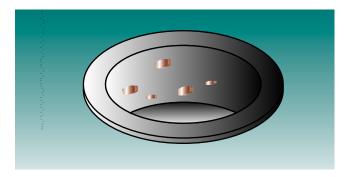


Figure 254c

### Acceptable - Class 1

- No more than five voids in any hole.
- Not more than 15% of the holes have voids.
- Any void is not more than 10% of the hole length.
- $\bullet$  All voids are less than  $90^{\circ}$  of the circumference.

### Nonconforming - Class 1, 2, 3

# 2.5.5 Lifted Lands - (Visual)



Figure 255a

# Target Condition/Acceptable - Class 1, 2, 3 • No lifting of lands.

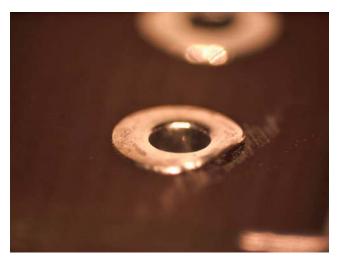


Figure 255b



Figure 255c

### Nonconforming - Class 1, 2, 3

# 2.5.6 Cap Plating of Filled Holes - (Visual)

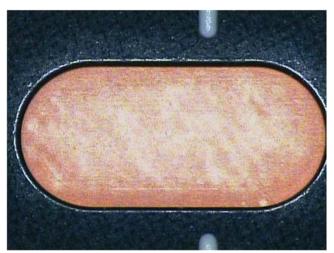


Figure 256a

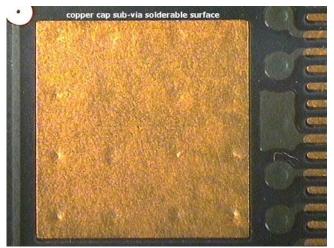


Figure 256b

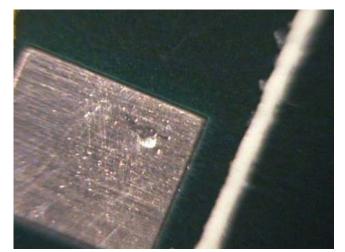


Figure 256c

### Target Condition - Class 1, 2, 3

• Copper surface is planar with no indication of cap plating.

### Acceptable - Class 1, 2, 3

- When cap plating of the filled via is specified on the procurement documentation, the requirements of 2.7.1.1 and the requirements of the applicable performance specification for rectangular and round surface mount pads shall apply.
- No plating voids exposing the resin fill area, unless covered by solder mask.
- Visually discernable protrusions (bumps) and/or depressions (dimples) that meet the microsection requirements of the applicable performance specification.

### 2.5 HOLES - PLATED-THROUGH - GENERAL

# 2.5.6 Cap Plating of Filled Holes - (Visual) (cont.)

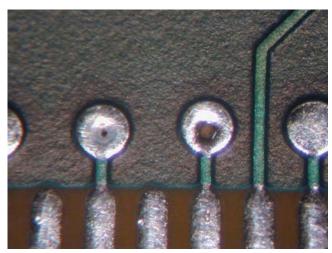
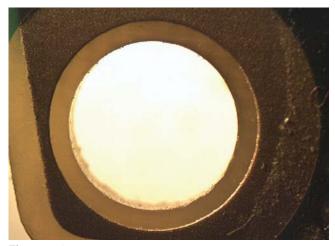


Figure 256d

### Nonconforming - Class 1, 2, 3

# 2.6.1 Haloing

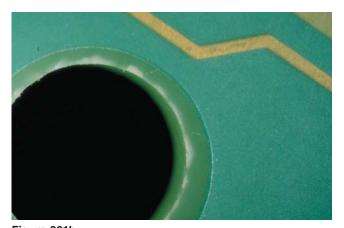
**Haloing:** Mechanically induced fracturing or delamination on or below the surface of the base material; a light area around the holes, other machined areas or both are usually indications of haloing. See also 2.1.3.



No haloing.

Target Condition - Class 1, 2, 3

Figure 261a



Acceptable - Class 1, 2, 3

 Distance between the haloing penetration and the nearest conductive feature is not less than the minimum lateral conductor spacing, or 100 µm [3,937 µin] if not specified.

Figure 261b



Nonconforming - Class 1, 2, 3

Figure 261c

# 2.7.1 Surface Plating - Plated Contacts

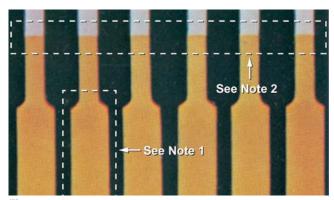


Figure 271a

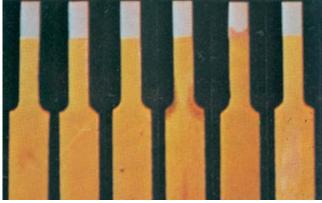


Figure 271b

### Target Condition - Class 1, 2, 3

- Contacts are free of pits, pinholes and surface nodules.
- No exposed copper or plating overlap between solder finish or solder mask and tip finish.

### Acceptable - Class 1, 2, 3 (Critical Contact Area)

- Surface defects do not expose underlying metal in critical contact area.
- Solder splashes or tin-lead plating does not occur in critical contact area.
- No nodules and metal bumps in critical contact area.
- Pits, dents or depressions do not exceed 0.15 mm [0.00591 in] in their longest dimension. There are not more than three per contact, and they do not appear on more than 30% of the contacts.

### Acceptable - Class 3 (Gap/Overlap Area)

• Exposed copper or plating overlap is 0.8 mm [0.031 in] or less.

### Acceptable - Class 2 (Gap/Overlap Area)

• Exposed copper or plating overlap does not exceed 1.25 mm [0.04921 in].

### Acceptable - Class 1 (Gap/Overlap Area)

• Exposed copper or plating overlap does not exceed 2.5 mm [0.0984 in].

Note 1: Discoloration is permitted in the plating overlap zone.

**Note 2:** Critical Contact Area. These conditions do not apply to a band 0.15 mm [0.00591 in] wide around the periphery of the printed contact land.

# 2.7.1 Surface Plating - Plated Contacts (cont.)

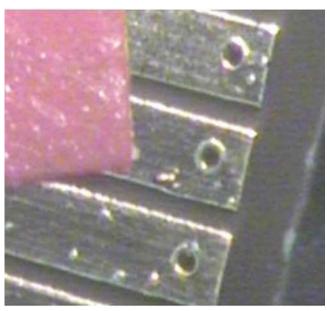


Figure 271c

### Nonconforming - Class 1, 2, 3

# 2.7.1.1 Surface Plating - Wire Bond Pads

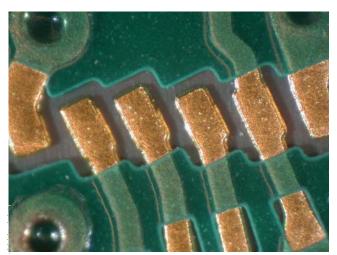


Figure 2711a

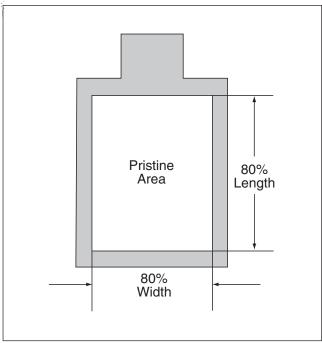


Figure 2711b Pristine Area

### Target Condition - Class 1, 2, 3

- Contacts are free of surface nodules, roughness, electrical test witness marks or scratches that exceed 0.8 µm [32 µin] RMS (root-mean-square) in the pristine area in accordance with an applicable test method AABUS. If IPC-TM-650, Method 2.4.15, is used, it is recommended that the roughness-width cutoff be adjusted to approximately 80% of the maximum length of the wire bond pad in order to obtain the RMS value within the pristine area. For more information on surface roughness, refer to ASME B46.1.
- The pristine area is defined as an area bounded in the center of the pad by 80% of the pad width and 80% of the pad length (see Figure 2711b).

# 2.7.1.1 Surface Plating - Wire Bond Pads (cont.)

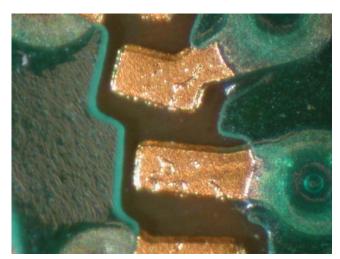


Figure 2711c

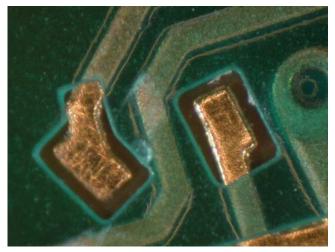


Figure 2711d

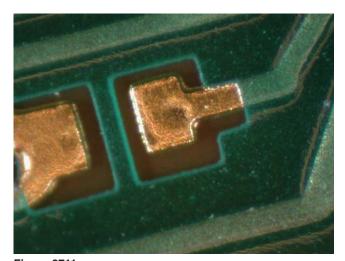


Figure 2711e

# 2.7.2 Burrs on Edge-Board Contacts

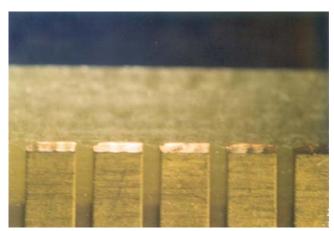


Figure 272a



Figure 272b

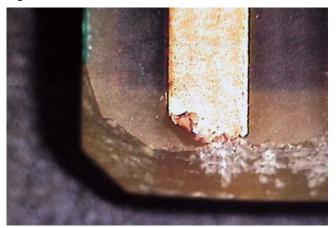


Figure 272c

### Target Condition - Class 1, 2, 3

• Smooth edge condition.

### Acceptable - Class 1, 2, 3

 Edge condition - smooth, no burrs, no rough edges, no lifted plating on printed contacts, no separation (delamination) of printed contacts from the base material, and no loose fibers on the beveled edge. Exposed copper at end of printed contact is expected and permissible.

### Nonconforming - Class 1, 2, 3

# 2.7.3 Adhesion of Overplate

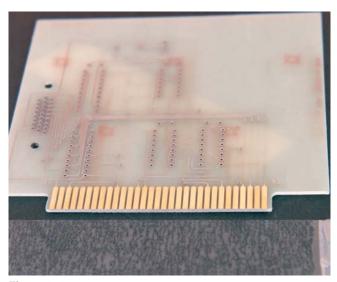


Figure 273a

### Target/Acceptable - Class 1, 2, 3

Good plating adhesion as evidenced by tape test. No plating removed. If overhanging metal breaks off and adheres to the tape, it is evident of overhang or slivers, but not of plating adhesion failure. Figure 273b provides an example of overhanging metal.

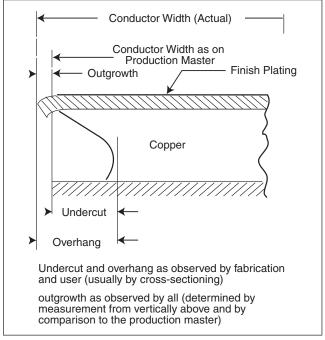


Figure 273b

### Nonconforming - Class 1, 2, 3

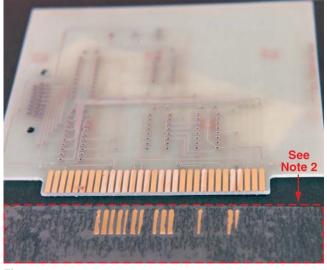


Figure 273c

- **Note 1:** The adhesion of the plating **shall** be tested in accordance with IPC-TM-650, Method 2.4.1, using a strip of pressure sensitive tape applied to the surface and removed by manual force applied perpendicular to the circuit pattern.
- Note 2: Plating that has adhered to the tape.

## Introduction

This section covers acceptability criteria for marking of printed boards. Marking of printed boards provides a means of identification and aids in assembly. Legends screened over metal will generally degrade in a solder process or stringent cleaning environments. Legends over metal are not recommended. When use of legends over solderable surfaces is required, an etched legend is target condition. Minimum requirements should be specified on the procurement documentation. Examples of the marking addressed by this section are:

- Assembly or fabrication part numbers when a requirement of the procurement documentation. Each individual board, each
  qualification board, and each set of quality conformance test circuitry (as opposed to each individual coupon) shall be marked
  in order to ensure traceability between the boards/test circuitry and the manufacturing history and to identify the supplier (logo,
  etc.).
- Component insertion locators, when a requirement of the procurement documentation.
- Manufacturing sequence number when required by the work order.
- Revision letter when the part number is a requirement of the procurement documentation.
- Designator for test points or adjustment points.
- Polarity or clocking indicators.
- U.L. designator.

The procurement documentation (artwork) is the controlling document for location and type of marking. The procurement documentation revision letter to which the printed board is fabricated **shall** be marked on the board if part number marking is a requirement of the procurement documentation. Marking on printed boards **shall** withstand all tests, cleaning and compatible processes to which the printed boards are subjected and **shall** be legible (capable of being read and understood) as defined by the requirements of this document. If a conductive marking is used, the marking **shall** be treated as a conductive element on the printed board and **shall** conform to IPC-4781.

The marking information on printed boards (part reference designations), **shall** be permanent and be capable of withstanding the environmental tests and cleaning procedures specified for the printed board. Marking **shall** be legible within the requirement of this document. The board **shall** be inspected at no greater magnification than 2X. When conductive inks are used they should meet the specifications of the IPC-6010 series.

This section has general requirements for all marking (including laser, labels, bar coding, etc.) and specific criteria for the following types of marking:

- Etched Markings.
- Screened or Ink Stamped Markings.

Unless otherwise specified, each individual printed board, each qualification board, each set of quality conformance test circuitry (as opposed to each individual coupon) is marked in accordance with the procurement documentation, with the date code and manufacturer's identification (e.g., cage code for military, logo, etc.). The marking is produced by the same process as used in producing the conductive pattern, or by use of permanent fungistatic ink or paint, or by vibrating pencil marking on a metallic area provided for marking purposes or a permanently attached label. Conductive markings, either etched copper or conductive black ink are considered as electrical elements of the printed board and should not reduce the electrical spacing requirements. All markings are to be compatible with materials and parts, legible for all tests, and in no case affect board performance.

Although it is acceptable to use impression stamp markings on unused portions of panels, they are not allowed on finished printed boards. Engraved marking or impression stamps and any mark that cuts into the laminate is handled in the same manner as a scratch.

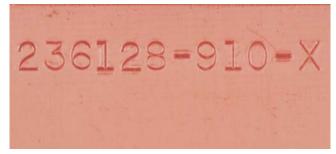


Figure 28a

# 2.8.1 Etched Marking

An etched marking is produced the same as the conductors on the printed board. As a result, the following criteria **shall** be met for etched marking:



Figure 281a



Figure 281b

### Target Condition - Class 1, 2, 3

- Characters are legible.
- Minimum conductor spacing requirements have also been maintained between etched symbolization and active conductors.

### Acceptable - Class 3

- Marking defects regardless of cause, (i.e., solder bridging, overetching, etc.) as long as characters are legible.
- Marking does not violate the minimum electrical clearance limits.
- Edges of the lines forming a character may be slightly irregular.

### Acceptable - Class 2

- Marking defects regardless of cause, (i.e., solder bridging, overetching, etc.) as long as characters are legible.
- Marking does not violate the minimum electrical clearance limits.
- Width of the lines forming a character may be reduced by up to 50%, providing they remain legible.

# 2.8.1 Etched Marking (cont.)



Figure 281c

### Acceptable - Class 1

- Marking defects regardless of cause, (i.e., solder bridging, overetching, etc.) as long as characters are legible.
- Marking does not violate the minimum electrical clearance limits.
- Legends are irregularly formed but the general intent of the legend or marking is legible.



Figure 281d

### Nonconforming - Class 1, 2, 3

# 2.8.2 Screened or Ink Stamped Marking

Screened or ink stamped marking refers to any type of marking that is printed on top of the printed board. No cutting or etching is involved in producing this type of marking.



Figure 282a

### Target Condition - Class 1, 2, 3

- Characters are legible.
- Ink distribution is uniform, with no smearing or double images.
- Ink markings are no closer than tangent to a land.

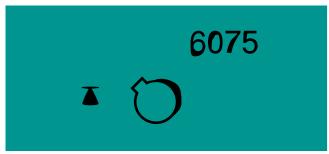


Figure 282b



Figure 282c

### Acceptable - Class 2, 3

- Characters are legible.
- Ink may be built up outside the character line providing the character is legible.
- Portion of component clocking symbol outline in the Figure 282c example may be missing, providing the required clocking is clearly defined.
- Marking ink on component hole land does not extend into the part mounting hole, or reduce minimum annular ring.
- Marking ink is allowed in PTHs and via holes into which no component lead is soldered unless the procurement document requires that the holes be completely solder filled.
- No encroachment of marking ink on edge board printed contacts or test points.
- On surface mount lands with a pitch of 1.25 mm [0.04921 in] or greater, encroachment of marking ink is on one side of land only and does not exceed 0.05 mm [0.0020 in].
- On surface mount lands with a pitch less than 1.25 mm [0.04921 in], encroachment of marking ink is on one side of land only and does not exceed 0.025 mm [0.000984 in].

# 2.8.2 Screened or Ink Stamped Marking (cont.)



Figure 282d

### Acceptable - Class 1

- Characters are legible.
- Ink may be built up outside the character line providing the character is legible.
- Portion of component clocking symbol outline in the Figure 282c example may be missing, providing the required clocking is clearly defined.
- Marking ink on component hole land does not extend into the part mounting hole, or reduce minimum annular ring.
- Marking ink is allowed in PTHs and via holes into which no component lead is soldered unless the procurement document requires that the holes be completely solder filled.
- No encroachment of marking ink on edge board printed contacts or test points.
- On surface mount lands with a pitch of 1.25 mm [0.04921 in] or greater, encroachment of marking ink is on one side of land only and does not exceed 0.05 mm [0.0020 in].
- On surface mount lands with a pitch less than 1.25 mm [0.04921 in], encroachment of marking ink is on one side of land only and does not exceed 0.025 mm [0.000984 in].
- Marking may be smeared or blurred provided it is still legible.
- Double images are legible.

### Nonconforming - Class 1, 2, 3

### 2.9 SOLDER MASK

### Introduction

The term "Solder Mask" is used in this document as a general term when referring to any type of permanent polymer coating material used on printed boards. Solder masks are used to limit and control the application of solder to selected areas of the printed board during assembly soldering operations. Solder mask coatings are used to control and limit surface contamination of printed board surfaces during soldering and subsequent processing operations, and are sometimes used to reduce dendritic filament growth(s) between conductive patterns over the printed board base material surface. Detailed specifications and information regarding solder mask requirements are contained in IPC-6012 and IPC-SM-840.

Solder mask materials are not intended for use as a substitute for conformal coatings that are applied after assembly to cover components, component lead/terminations and solder connections. Determination of compatibility of solder mask materials with conformal coating materials, or other substances, is dependent upon the end item assembly environments.

Solder mask thickness cannot be visually determined. If solder mask thickness is specified, microsectional analysis is required and evaluated per 3.3.12.

The types of solder mask include:

- Deposited image, (liquid) screen printed form.
- Deposited image, electrostatic.
- Photo defined image, (liquid) form.
- Photo defined image, (dry film) form.
- Photo defined image, temporary mask.
- Photo defined, dry film over liquid.

**Note:** Touch up, if required to cover these areas with solder mask, **shall** be of a material that is compatible to and of equal resistance to soldering and cleaning as the originally applied mask.

# 2.9.1 Coverage Over Conductors (Skip Coverage)

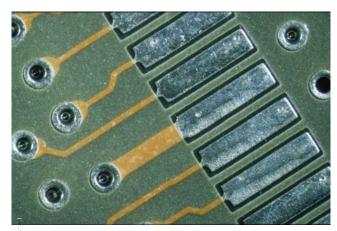


Figure 291a



Figure 291b

### Target Condition - Class 1, 2, 3

 The solder mask exhibits uniform appearance over the base material surface, conductor sides and edges. It is firmly bonded to the printed board surface with no visible skipping, voids or other defects.

### Acceptable - Class 2, 3

- In areas containing parallel conductors, adjacent conductors are not exposed by the absence of solder mask except where space between conductors is intended to be exposed.
- Touch up, if required to cover these areas with solder mask, is of a material that is compatible to and of equal resistance to soldering and cleaning as the originally applied solder mask.

### Acceptable - Class 1

- The missing solder mask does not reduce the conductor spacing between conductive patterns below the minimum acceptability requirements.
- There is skipping of the solder mask along the sides of the conductive patterns.

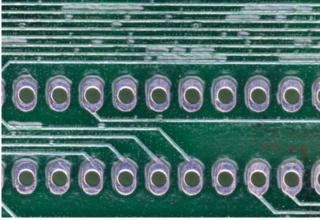
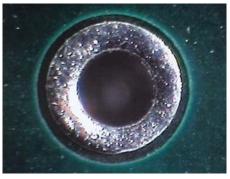


Figure 291c

### Nonconforming - Class 1, 2, 3

# 2.9.2 Registration to Holes (All Finishes)



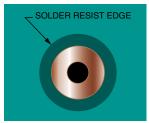


Figure 292b

### Target Condition - Class 1, 2, 3

 No solder mask misregistration. The solder mask is centered around the lands within the nominal registration spacings.





Figure 292c

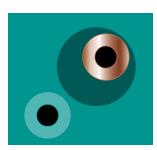


Figure 292d

### Acceptable - Class 1, 2, 3

- Misregistration of the mask to the land patterns but the solder mask does not violate minimum annular ring requirements.
- No solder mask in PTHs, except those not intended for soldering.
- Adjacent, electrically isolated lands or conductors are not exposed.

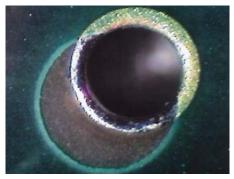


Figure 292e

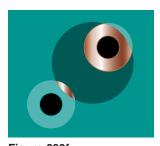


Figure 292f

### Nonconforming - Class 1, 2, 3

# 2.9.3 Registration to Other Conductive Patterns

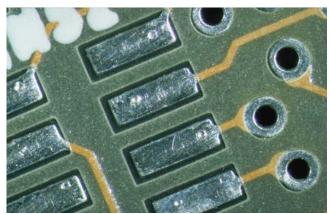


Figure 293a

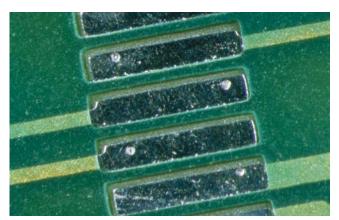


Figure 293b

# Target Condition - Class 1, 2, 3

• No solder mask misregistration.

### Acceptable - Class 1, 2, 3

- Misregistration to copper-defined lands does not expose adjacent, electrically isolated lands or conductors.
- No solder mask encroachment on edge board printed contacts or test points.
- On surface mount lands with a pitch of 1.25 mm [0.04921 in] or greater, encroachment is on one side of land only and does not exceed 0.05 mm [0.0020 in].
- On surface mount lands with a pitch less than 1.25 mm [0.04921 in], encroachment is on one side of land only and does not exceed 0.025 mm [0.000984 in].

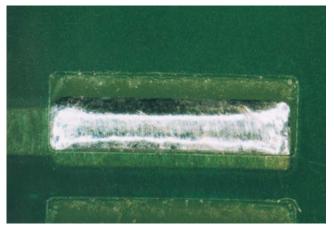
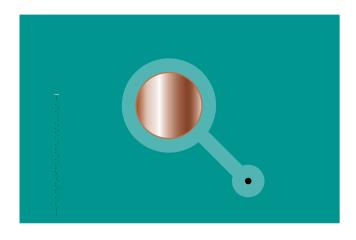


Figure 293c

### Nonconforming - Class 1, 2, 3

# 2.9.3.1 Ball Grid Array (Solder Mask-Defined Lands)

**Solder Mask-Defined Lands:** A portion of the conductive pattern, used to connect electronic component ball terminations, (BGAs, Fine-Pitch BGAs, etc.), where the solder mask encroaches on the edges of the land to restrict the ball attachment within the solder mask profile.



### Target Condition - Class 1, 2, 3

• The solder mask overlap is centered around the lands.



Figure 2931a

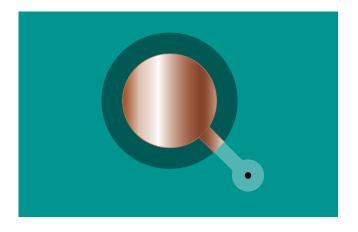
### Acceptable - Class 1, 2, 3

• Misregistration creates breakout of the solder mask on the land of not more than 90°.

### Nonconforming - Class 1, 2, 3

# 2.9.3.2 Ball Grid Array (Copper-Defined Lands)

**Copper-Defined Lands:** A portion of the conductive pattern usually, but not exclusively, used for the connection and/or attachment of components where the land metal is involved in the attachment process, and if solder mask is applied to the product a clearance is provided for the land area.



### Target Condition - Class 1, 2, 3

• The solder mask is centered around the copper land with clearance.



Figure 2932a



Figure 2932b

### Acceptable - Class 1, 2, 3

 Solder mask does not encroach on the land, except at the conductor attachment.

### Nonconforming - Class 1, 2, 3

### 2.9 SOLDER MASK

# 2.9.3.3 Ball Grid Array (Solder Dam)

**Solder Dam:** A portion of the solder mask pattern, used in conjunction with BGA or Fine Pitch BGA mounting, that provides a segment of solder mask material to separate the mounting portion of the pattern and the interconnection via in order to avoid solder being skived from the attachment joint into the via.

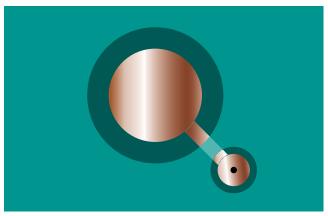


Figure 2933a

### Target Condition - Class 1, 2, 3

• The solder mask is centered around the copper land and escape via with clearance. Mask only covers the conductor between copper land and escape via.

### Acceptable - Class 1, 2, 3

• If solder mask dam is specified (to prevent bridging of solder to the via), it remains in place with the copper covered.

### Nonconforming - Class 1, 2, 3

# 2.9.4 Blisters/Delamination

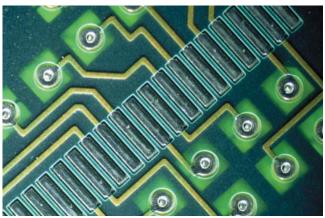


Figure 294a

### Target Condition - Class 1, 2, 3

 No evidence of blisters, bubbles or delamination between the solder mask and the printed board base material and conductive patterns.

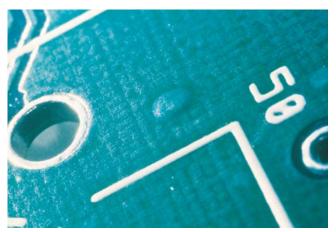


Figure 294b

# Acceptable - Class 2, 3 Two per side not exceeding 0.25 mm [0.0984 in] in the greatest dimension. Reduction of electrical spacing does not exceed 25%, or the minimum spacing.

### Acceptable - Class 1

• Blisters, bubbles or delamination do not bridge between conductors.

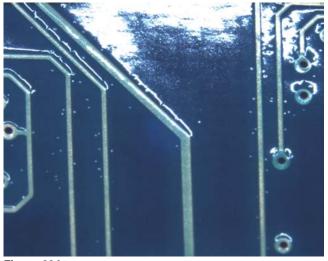


Figure 294c

### 2.9 SOLDER MASK

# 2.9.4 Blisters/Delamination (cont.)

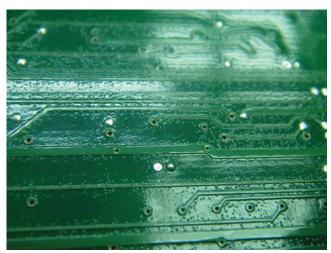


Figure 294d

### Nonconforming - Class 1, 2, 3

# 2.9.5 Adhesion (Flaking or Peeling)

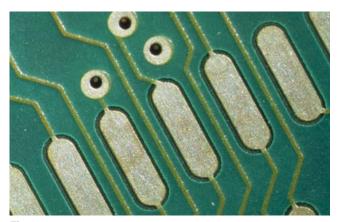


Figure 295a

### Target Condition - Class 1, 2, 3

• The surface of the solder mask is uniform in appearance and is firmly bonded to the printed board surfaces.

### Acceptable - Class 2, 3

- No evidence of solder mask lifting from the printed board prior to testing.
- After testing in accordance with IPC-TM-650, Method 2.4.28.1, the amount of solder mask lifting does not exceed the allowable limits of the IPC-6010 Series.

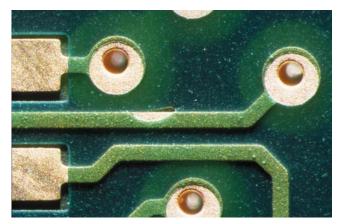


Figure 295b

### Acceptable - Class 1

- Prior to testing, the solder mask is flaking from the printed board base material or conductive pattern surfaces and the remaining solder mask is firmly bonded. The missing solder mask does not expose adjacent conductive patterns or exceed allowable lifting.
- After testing in accordance with IPC-TM-650, Method 2.4.28.1, the amount of solder mask lifting does not exceed the allowable limits of the IPC-6010 Series.

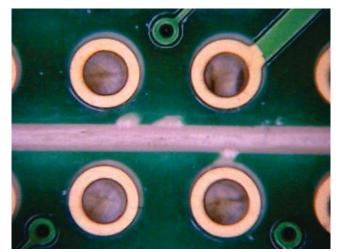


Figure 295c

### Nonconforming - Class 1, 2, 3

# 2.9.6 Waves/Wrinkles/Ripples

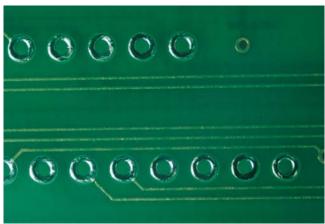


Figure 296a

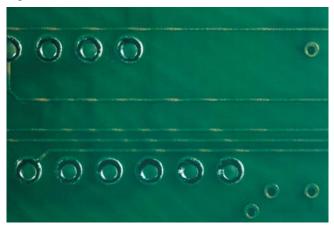


Figure 296b



Figure 296c

### Target Condition - Class 1, 2, 3

• There are no wrinkles, waves, ripples or other defects in the solder mask coating over the printed board base material surfaces or conductive patterns.

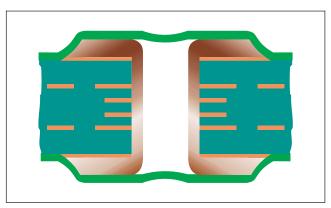
### Acceptable - Class 1, 2, 3

- Waves or ripples in the solder mask do not reduce the solder mask coating thickness below the minimum thickness requirements (when specified).
- Wrinkling is located in an area that does not bridge conductive patterns and passes IPC-TM-640, Method 2.4.28.1 (adhesion tape pull test).

### Nonconforming - Class 1, 2, 3

# 2.9.7 Tenting (Via Holes)

Tenting refers to a via with a mask material applied bridging over the via wherein no additional materials are in the hole. It may be applied to one side or both sides of the via structure (see Figure 297a), though single sided tenting is not recommended.



### Figure 297a

Note: This graphic is for illustrative purposes only and does not require a microsection evaluation.

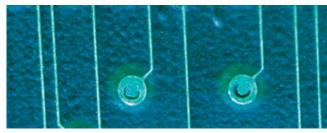


Figure 297b

### Target Condition - Class 1, 2, 3

 All holes required to be tented are completely covered with mask.

### Acceptable - Class 1, 2, 3

• All holes required to be tented are covered by mask.

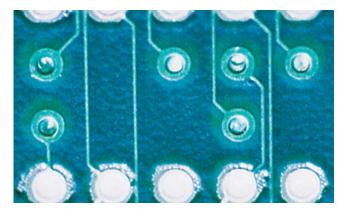


Figure 297c

### Nonconforming - Class 1, 2, 3

# 2.9.8 Soda Strawing

**Soda Strawing:** A long tubular-like void along the edges of conductive patterns where the solder mask is not bonded to the base material surface or the edge of the conductor. Tin/lead fusing fluxes, fusing oils, solder fluxes, cleaning agents or volatile materials may be trapped in the soda straw void.



Figure 298a

### Target Condition - Class 1, 2, 3

 No visible soda straw voids between the solder mask and the printed board base material surface and the edges of the conductive patterns.



Figure 298b

### Acceptable - Class 3

• No evidence of soda strawing.

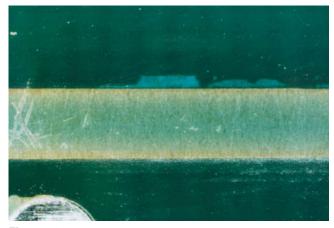


Figure 298c

### Acceptable - Class 1, 2

- Soda strawing along side conductive pattern edges does not reduce the conductor spacing below the minimum requirements.
- Soda strawing is completely sealed from the external environment.



Figure 298d

### 2.9 SOLDER MASK

# 2.9.8 Soda Strawing (cont.)

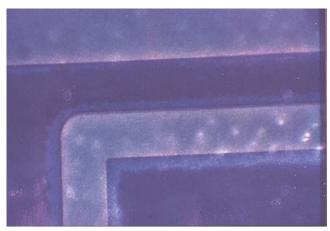


Figure 298e

### Nonconforming - Class 1, 2, 3



Figure 298f

### 2.10 PATTERN DEFINITION - DIMENSIONAL

### Introduction

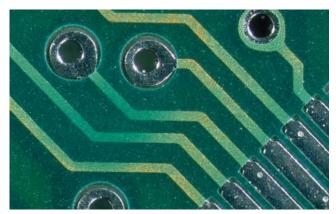
Printed boards **shall** meet the dimensional requirements specified on the procurement documentation such as printed board periphery, thickness, cutouts, slots, notches and printed board edge contacts. The accuracy, repeatability and reproducibility of the equipment used to verify the characteristics of printed boards should be 10% or less of the tolerance range of the dimensions being verified.

# 2.10.1 Conductor Width and Spacing

This section covers acceptability requirements and criteria for conductor width and spacing. Acceptable conductor width and spacing is a measure of how well the printed board fabrication process is reproducing the master image, which basically determines the width and spacing requirements for the conductive patterns. Unless these characteristics are violated, edge definition itself is not necessarily a characteristic for acceptance or nonconformance; however, it can be considered a process indicator, requiring review of manufacturing procedures. In addition it may be an important consideration for controlled impedance circuits. Procurement documentation should establish edge definition requirements for applications of these types. When required, measurements of conductor edge definition are made in accordance with IPC-TM-650, Method 2.2.2.

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# 2.10.1.1 Conductor Width



Target Condition - Class 1, 2, 3

• Conductor width meets dimensional requirements of artwork or procurement documentation.

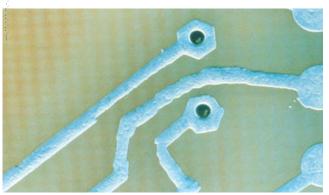
Figure 21011a



Acceptable - Class 2, 3

- Any combination of isolated edge roughness, nicks, pinholes, and scratches exposing base material that reduces the conductor width by 20% of the minimum value or less.
- There is no occurrence (edge roughness, nicks, etc.) greater than 10% of the conductor length or more than 13.0 mm [0.512 in], whichever is less.

Figure 21011b



Acceptable - Class 1

- Any combination of isolated edge roughness, nicks, pinholes, and scratches exposing base material that reduces the conductor width 30% of the minimum value or less.
- There is no occurrence (edge roughness, nicks, etc.) greater than 10% of the conductor length or more than 25.0 mm [0.984 in], whichever is less.

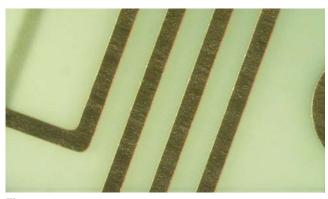
Figure 21011c



Nonconforming - Class 1, 2, 3

Figure 21011d

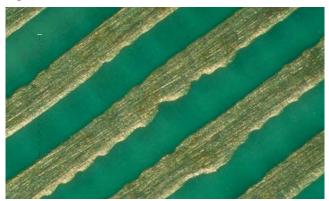
# 2.10.1.2 Conductor Spacing



Target Condition - Class 1, 2, 3

• Conductor spacing meets dimensional requirements of the procurement documentation.

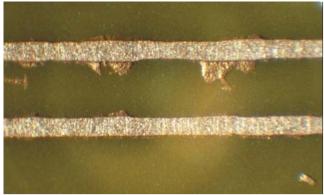
Figure 21012a



Acceptable - Class 3

• Any combination of edge roughness, copper spikes, etc., that does not reduce the specified minimum conductor spacing by more than 20% in isolated areas.

Figure 21012b



Acceptable - Class 1, 2

 Any combination of edge roughness, copper spikes, etc., that does not reduce the specified minimum conductor spacing by more than 30% in isolated areas.

Figure 21012c



Nonconforming - Class 1, 2,3

Figure 21012d

### 2.10 PATTERN DEFINITION - DIMENSIONAL

# 2.10.2 External Annular Ring - Measurement

**External Annular Ring:** The minimum annular ring on external layers is the minimum amount of copper (at the narrowest point) between the edge of the hole and the edge of the land after plating of the finished hole (see Figure 2102a). Hole breakout refers to a condition where a hole is not completely surrounded by the land (see Figure 2102b).

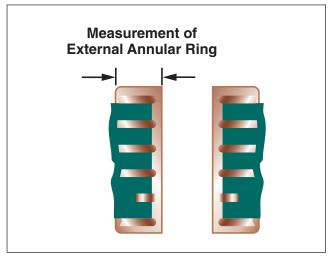


Figure 2102a External Annular Ring

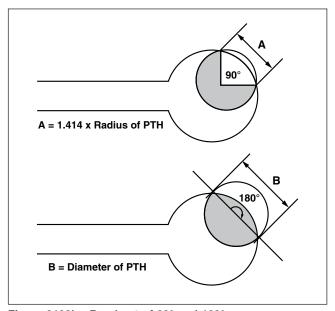


Figure 2102b Breakout of 90° and 180°

**Conductor to Land Junction:** A 90° area centered around the point where the conductor connects to the land (see Figure 2102c). This area only applies to breakout conditions (see Figure 2102d).

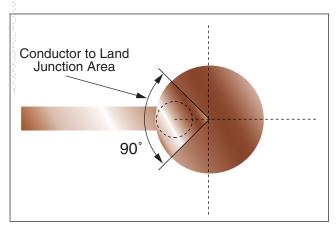


Figure 2102c Conductor to Land Junction

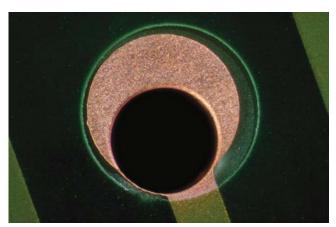


Figure 2102d Breakout at Conductor to Land Junction

# 2.10.3 External Annular Ring - Supported Holes

**Supported Hole:** A hole within a printed board that has its inside surfaces plated or otherwise reinforced.

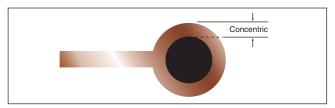


Figure 2103a

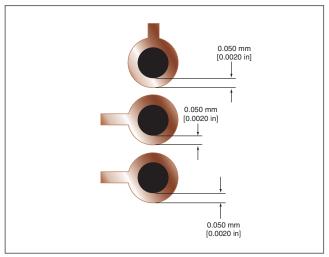


Figure 2103b

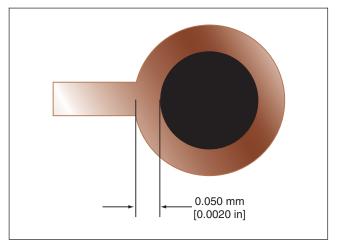


Figure 2103c

### Target Condition - Class 1, 2, 3

• Holes are centered in the lands.

### Acceptable - Class 3

- Holes are not centered in the lands, but the annular ring measures 0.050 mm [0.0020 in] or more.
- The minimum external annular ring may have 20% reduction of the minimum annular at the measurement area due to defects such as pits, dents, nicks, pinholes, or splay.

### 2.10 PATTERN DEFINITION - DIMENSIONAL

# 2.10.3 External Annular Ring - Supported Holes (cont.)

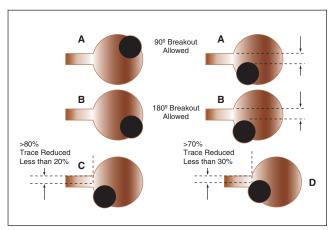


Figure 2103d

### Acceptable - Class 2

- 90° breakout or less (see item A in Figure 2103d).
- If breakout occurs at the conductor to land junction area, the land/conductor junction is not reduced by more than 20% of the minimum conductor width specified on the engineering drawing or the production master nominal. The conductor junction should never be less than 0.050 mm [0.0020 in] or the minimum line width, whichever is smaller (see item C in Figure 2103d).
- Minimum lateral spacing is maintained.

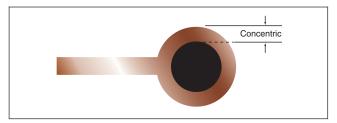
### Acceptable - Class 1

- 180° breakout or less (see item B in Figure 2103d).
- If breakout occurs at the conductor to land junction area, the conductor is not reduced by more than 30% of the minimum conductor width specified on the production master nominal (see item D in Figure 2103d).
- Form, fit and function are not affected.
- · Minimum lateral spacing is maintained.

### Nonconforming - Class 1, 2, 3

# 2.10.4 External Annular Ring - Unsupported Holes

Unsupported Hole: A hole within a printed board that does not contain plating or other type of conductive reinforcement.



### Figure 2104a

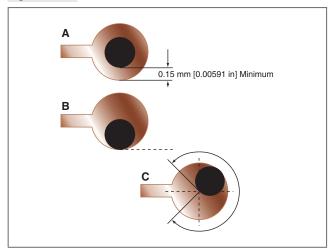


Figure 2104b

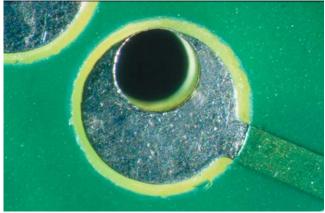


Figure 2104c

### Target Condition - Class 1, 2, 3

• Holes are centered in the lands.

### Acceptable - Class 3

 Annular ring measures 0.15 mm [0.00591 in] or more in any direction. (See item A in Figure 2104b) The minimum external annular ring may have a 20% reduction of the minimum annular ring at the measurement area due to defects such as pits, dents, nicks, pinholes or splay.

### Acceptable - Class 2

- 90° breakout is allowed. (See item B in Figure 2104b.)
- If breakout occurs at the conductor to land junction area, the conductor is not reduced by more than 20% of the minimum conductor width specified on the engineering drawing or the production master nominal.

### Acceptable - Class 1

- 90° breakout is allowed. (See item C in Figure 2104b.)
- If breakout occurs at the conductor to land junction area, the conductor is not reduced by more than 30% of the minimum conductor width specified on the production master nominal.

### Nonconforming - Class 1, 2, 3

#### 2.11 Flatness

### 2.11 Flatness

Flatness of printed boards is determined by two characteristics of the product; these are known as bow and twist. The bow condition is characterized by a roughly cylindrical or spherical curvature of the printed board while its four corners are in the same plane (see Figure 211a). Twist is the printed board deformation parallel to the diagonal of the printed board such that one corner is not in the same plane to the other three (see Figure 211b). Circular or elliptical printed boards must be evaluated at the highest point of vertical displacement. Bow and twist may be influenced by the printed board design as different circuit configurations or layer construction of multilayer printed boards can result in different stress or stress relief conditions. Printed board thickness and material properties are other factors that influence the resulting printed board flatness.

**Bow and Twist** Bow, twist, or any combination thereof, **shall** be determined by physical measurement and percentage calculation in accordance with IPC-TM-650, Method 2.4.22. End products **shall** be assessed in the delivered form.

### 2.11 Flatness (cont.)

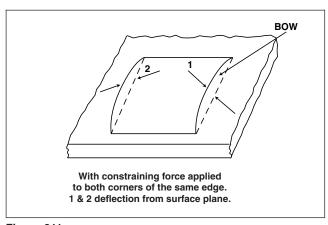


Figure 211a

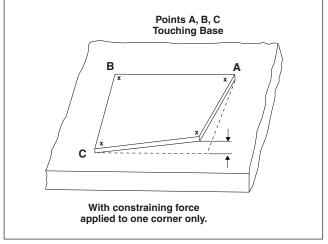


Figure 211b

#### Acceptable - Class 1, 2, 3

- For printed boards using surface mount components, the bow and twist **shall** be 0.75% or less.
- For all other printed boards, bow and twist **shall** be 1.50% or less.

### Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

#### **3 INTERNALLY OBSERVABLE CHARACTERISTICS**

### Introduction

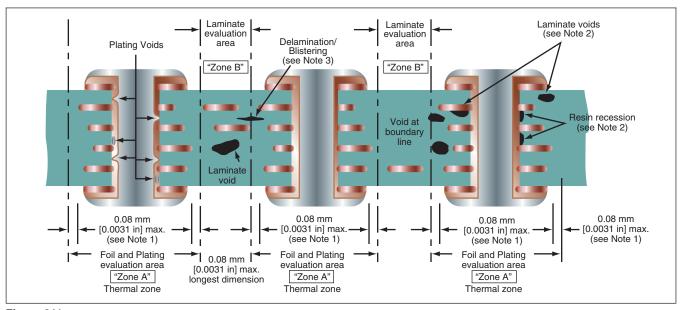
The purpose of this section is to provide acceptability requirements for those characteristics which are internal to the printed board. These include the following characteristics in the base material, PTHs, internal conductive copper pattern, treatments to the internal copper, and internal ground/power/thermal planes, as described below:

- Subsurface imperfections in printed board material, such as delamination, blistering, and foreign inclusions.
- Subsurface imperfections to multilayer printed boards, such as voids, delamination, blistering, cracks, ground plane clearance and layer to layer spacing.
- PTH anomalies, including size, annular ring, nailheading, plating thickness, plating voids, nodules, cracks, resin smear, inadequate or excessive etchback, wicking, inner layer (post) separation, and solder mask thickness.
- Internal conductor anomalies, such as over or under etch, conductor cracks and voids, uneven or inadequate oxide treatment, and foil thickness.
- Visual observations made on cross-sections only.

### Introduction

This section covers the acceptability requirements of dielectric materials. Dielectric materials are evaluated after thermal stress. Requirements for evaluations made in the as received condition should be stated on the procurement documentation.

### 3.1.1 Laminate Voids/Cracks (Outside Thermal Zone)



### Figure 311a

#### Notes:

- 1. The thermal zone extends 0.08 mm [0.0031 in] beyond the end of the land, either internal or external, extending furthest into the laminate area.
- 2. Laminate anomalies or imperfections that exist entirely in the Zone A area are not evaluated on specimens which have been exposed to thermal stress or rework simulation. Boundary line voids/cracks that overlap Zone A and Zone B as shown in Figure 311e or are entirely in Zone B **shall** meet the requirements of 3.1.1.
- 3. Delamination/Blistering is evaluated in both Zone A and Zone B.
- 4. Laminate anomalies or imperfections in the non-evaluation areas (at either end of the microsection specimen) are not evaluated on specimens which have been exposed to thermal stress or rework simulation.

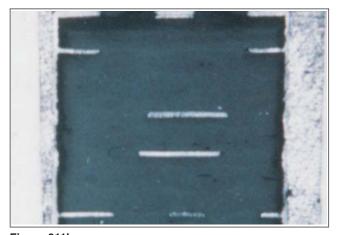


Figure 311b

#### Target Condition - Class 1, 2, 3

• Uniform and homogeneous laminate.

### 3.1.1 Laminate Voids/Cracks (Outside Thermal Zone) (cont.)

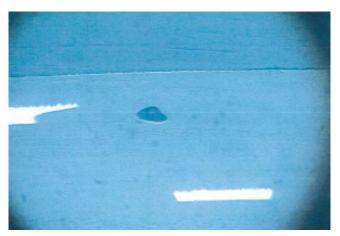


Figure 311c

#### Acceptable - Class 2, 3

- Void/crack less than or equal to 0.08 mm [0.0031 in] and does not violate minimum dielectric spacing.
- Laminate anomalies or imperfections, such as voids/cracks or resin recession, in Zone A areas that have been exposed to thermal stress and rework simulation.
- Multiple voids/cracks between two adjacent plated-through holes in the same plane that do not have combined length which exceeds these limits.

### Acceptable - Class 1

- Void/crack less than or equal to 0.15 mm [0.00591 in] and does not violate minimum dielectric spacing.
- Laminate anomalies or imperfections, such as voids/cracks or resin recession, in Zone A areas that have been exposed to thermal stress and rework simulation.
- Multiple voids/cracks between two adjacent plated-through holes in the same plane that do not have combined length which exceeds these limits.

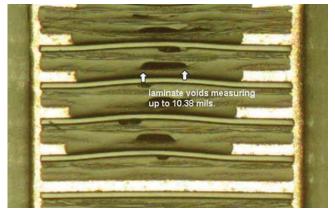


Figure 311d

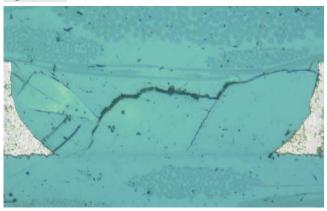


Figure 311e

Visual observations made on cross-sections only.

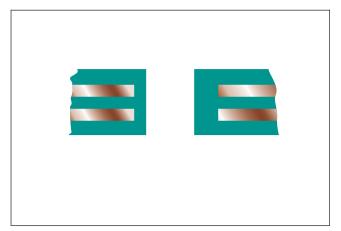
#### Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

## 3.1.2 Registration/Conductor to Holes

Registration of conductors is typically determined with respect to PTH lands. Requirements are established through minimum internal annular ring (see 3.3.1).

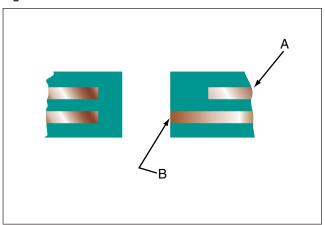
## 3.1.3 Clearance Hole, Unsupported, to Power/Ground Planes



#### Target Condition - Class 1, 2, 3

• Power/Ground plane setback meets the procurement documentation requirements.

Figure 313a



#### Acceptable - Class 1, 2, 3

- A) Power/ground plane setback is greater than the minimum electrical conductor spacing specified on the procurement documentation.
- B) Ground plane may extend to the edge of an unsupported hole when specified in the procurement documentation.

Figure 313b

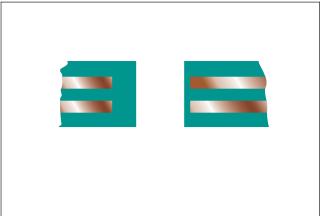


Figure 313c

### Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

### 3.1.4 Delamination/Blister



Figure 314a

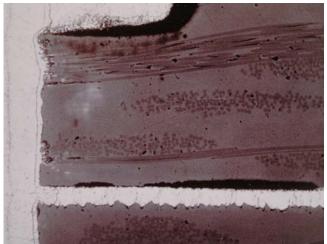


Figure 314b



Figure 314c

### Target Condition - Class 1, 2, 3

• No delamination or blistering.

#### Acceptable - Class 2, 3

• No evidence of delamination or blistering.

### Acceptable - Class 1

• If delamination or blistering is present, evaluate the entire printed board in accordance with 2.3.3.

#### Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

### 3.1.5 Etchback

Acceptable etchback or negative etchback exhibits the evidence that resin smear has been removed from the innerlayer copper/drilled hole interface. An example of resin smear appears in Figure 315a. There is data, pro and against, that etchback is more reliable than negative etchback and vice versa. This all depends on what type of copper plating, copper foil, and weight of the foil being used. Excessive etchback as well as excessive negative etchback are not the target condition. Excessive etchback, in both instances, has an adverse effect on the reliability of the PTH life.

**Etchback:** The etchback process, also known as positive etchback, is used to remove the dielectric material. The evidence of resin material being etched back theorizes that all resin smear has been removed and in addition, a three way interfacial bond occurs between the PTH copper to the innerlayer copper foil. The theory is that three connections are more reliable than one. The drawbacks of etchback are that it creates rough holes which could create PTH barrel cracks. Excessive etchback also contributes to stresses that might create foil cracks. Shadowing is defined as a condition that occurs during an etchback process in which the dielectric material immediately next to the foil is not removed completely. This can occur even though an acceptable amount of etchback may have been achieved elsewhere. Proper measurement locations for etchback are shown in Figure 315b.

**Negative Etchback:** The theory here is that in order for the internal foil to be etched back/cleaned, you need to eliminate the smear. The benefits for utilizing negative etchback are that the process does not create a stress point at the internal plane, as does the etchback process, and it results in a very smooth/uniform copper barrel hole wall. The smooth hole wall and negative etchback are beneficial especially for the copper plating of high-reliability long term life applications. The drawback of negative etchback, if excessive, is that it may create innerlayer separation due to entrapped air pockets/contamination. This section is not intended to prove or disprove which etchback process is preferred. There are many printed board manufacturers that are very successful in utilizing both the etchback and negative etchback processes. It is up to the individual designer/user, depending on the material, copper plating, copper foil and application, to specify which etchback process should be employed.

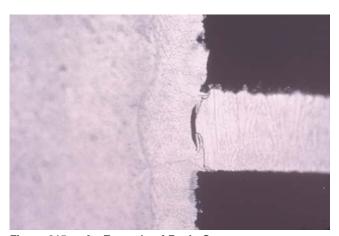


Figure 315a An Example of Resin Smear

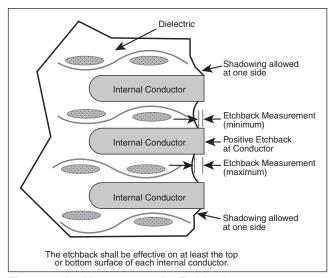


Figure 315b Measurement for Etchback

### 3.1.5.1 Etchback

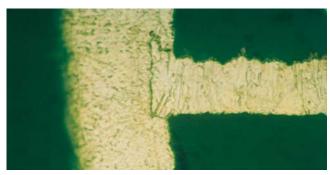


Figure 3151a

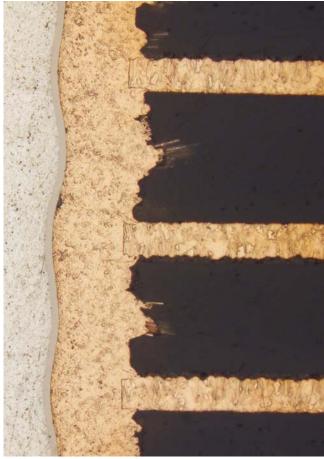


Figure 3151b

### Target Condition - Class 1, 2, 3

• Uniform etchback to a preferred depth of 0.013 mm [0.000512 in].

### Acceptable - Class 1, 2, 3

- Etchback between 0.005 mm [0.00020 in] and 0.08 mm [0.0031 in].
- Shadowing is permitted on one side only of each land.

# 3.1.5.1 Etchback (cont.)

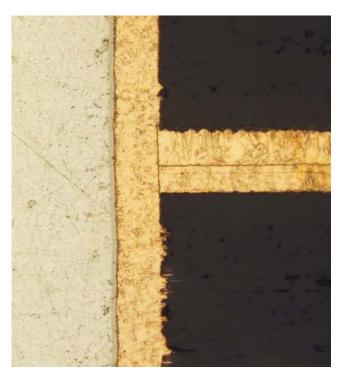


Figure 3151c



Figure 3151d

### Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

### 3.1.5.2 Negative Etchback



Figure 3152a

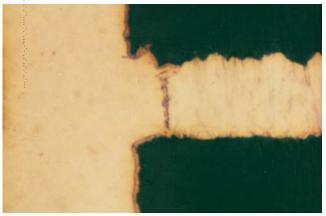


Figure 3152b



Figure 3152c

Visual observations made on cross-sections only.

#### Target Condition - Class 1, 2, 3

• Uniform negative etchback of copper foil 0.0025 mm [0.0000984 in].

#### Acceptable - Class 3

• Negative etchback less than 0.013 mm [0.000512 in].

#### Acceptable - Class 1, 2

• Negative etchback less than 0.025 mm [0.000984 in].

#### Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

### 3.1.6 Smear Removal

Smear removal is defined as the removal of resin debris which results from the formation of the hole wall.

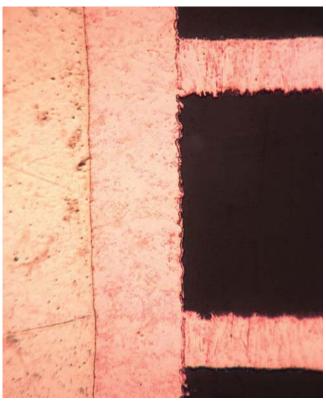


Figure 316a

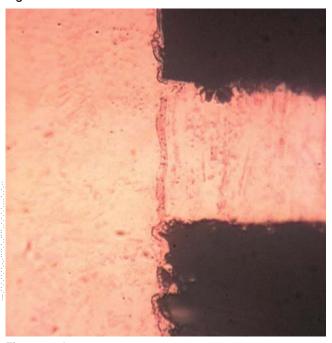


Figure 316b

#### Acceptable - Class 1, 2, 3

- Smear removal has not been etched back greater than 0.025 mm [0.001 in].
- Random tears or drill gouges producing small areas where the 0.025 mm [0.001 in] depth has been exceeded **shall** be evaluated as etchback per 3.1.5.1.
- Smear removal sufficiently meets the acceptability criteria for plating separation (3.3.14).

# 3.1.6 Smear Removal (cont.)



Figure 316c

### Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

### 3.1.7 Dielectric Material, Clearance, Metal Plane for Supported Holes

Metal planes are used for mechanical reinforcement and/or electromagnetic shielding for printed boards. Many requirements are the same as for metal-core printed boards.

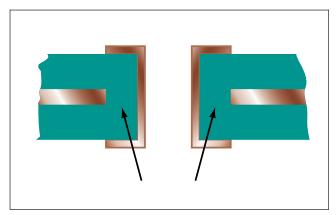


Figure 317a

Figure 317b

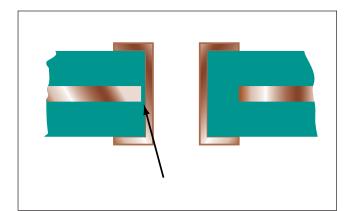


Figure 317c

#### Target Condition - Class 1, 2, 3

• Metal plane setback exceeds the procurement documentation requirements.

#### Acceptable - Class 1, 2, 3

- Metal plane setback is equal to or greater than 0.1 mm [0.0040 in] (when a value is not specified by the procurement documentation).
- Metal plane setback does not reduce the conductor spacing to less than the specified minimum on the procurement documentation.

#### Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

### 3.1.8 Layer-to-Layer Spacing

Minimum dielectric thickness is the maximum material condition used for the electrical voltage dielectric strength requirements.

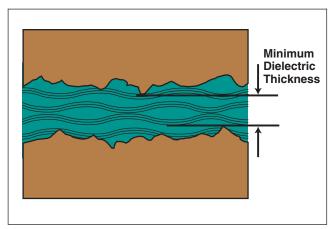


Figure 318a

#### Target Condition - Class 1, 2, 3

• The minimum dielectric thickness meets the requirements of the procurement documentation.

#### Acceptable - Class 1, 2, 3

- The minimum dielectric thickness meets the minimum requirements of the procurement documentation.
- If the minimum dielectric spacing and the number of reinforcing layers are not specified, the minimum dielectric spacing shall be 0.09 mm [0.0035 in] and the number of reinforcing layers shall be selected by the supplier.
- Low profile copper foils should be used with dielectrics below 0.09 mm [0.0035 in].

#### Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

### Notes:

- 1: Products designed for transmission line impedance applications may have special requirements and measurement method specified on procurement documentation.
- 2: When the nominal dielectric thickness on the drawing is less than 90  $\mu$ m [3,543  $\mu$ in], the minimum dielectric spacing is 25  $\mu$ m [984  $\mu$ in] and the number of reinforcing layers may be selected by the supplier.

### 3.1.9 Resin Recession

**Resin Recession:** A separation between the plated barrel of the hole and the dielectric material on the hole wall.

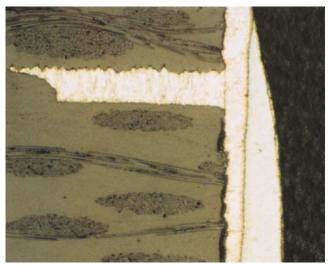


Figure 319a

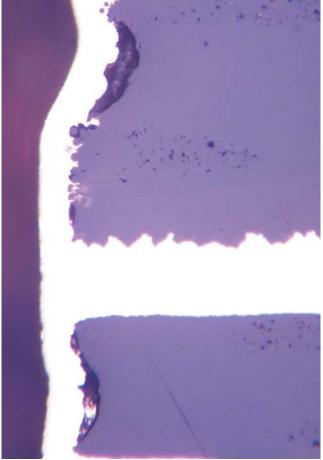


Figure 319b

Visual observations made on cross-sections only.

• Resin recession is acceptable following thermal stress testing.

## 3.1.10 Hole Wall Dielectric/Plated Barrel Separation (Hole Wall Pullaway)



### Acceptable - Class 1, 2, 3

• Dimensional and plating requirements of IPC-6010 performance series are met.

#### Figure 3110a

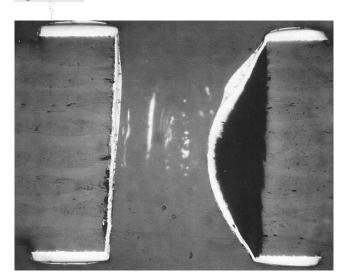


Figure 3110b

#### Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

#### 3.2 CONDUCTIVE PATTERNS - GENERAL

### Introduction

This section covers acceptability requirements for printed board etching, innerlayers, and impedance controlled products. An acceptable etching process must result in all residual metal being removed with no evidence of contamination remaining on the product.

Over etching is cause for rejection when potential slivers result from excessive overhang of metal resist plating or when the finished conductor widths are less than specification requirements.

Under etching is cause for rejection when spurious metal remains on the product to the extent that spacing between conductors is less than specification requirements or if conductor width requirements are exceeded.

Conductor width is defined as the observable width of the copper conductor excluding organic or metallic resists unless otherwise specified. The "Minimum Conductor Width" often specified on the procurement documentation or performance document is usually measured at the base of the conductor and may not be the actual narrowest width of the conductor when observed in cross section or often when viewed from the surface. An observation from the surface may not be adequate for acceptance of some products and etching processes. Where resistance per unit length is a requirement, a measurement of the average width of the cross-sectional area may be necessary. Where impedance control is required, a determination of the maximum conductor width may be important for the calculating impedance and a cross-section is often required.

Considerable variation in etch configurations is possible due to different etchants, resists and plated metal thicknesses. The conductor width may increase or decrease from the production artwork due to techniques used in processing during the imaging and developing operations. To achieve the "Design Width of Conductor," the production master artwork often has conductor width adjustments made during plotting. The amount of adjustment of a conductor width on the "Production Master" may be 0.025 to 0.05 mm [0.001 to 0.0020 in]. Determination of adjustment is made by experimentation and compensation for an increase or decrease of the conductor width during plating or etching.

The illustrations in 3.2.1 are intended as a guideline to illustrate some of the edge geometry conditions which may result from different processing methods and illustrate the configurations of "Outgrowth," "Undercut" and "Overhang."

Definitions used in evaluating etched conditions (see IPC-T-50) include:

**Outgrowth:** The increase in conductor width at one side of the conductor, caused by plating buildup over that delineated by the production master.

**Undercut:** The distance on one edge of the conductor measured parallel to the printed board surface from the outer edge of the conductor, including etch resists, to the maximum point indentation to the copper conductor.

Overhang: The sum of the outgrowth and undercut.

Design width of conductor: The width of a conductor as delineated or noted on the procurement documentation.

**Notes:** 1. The "Production Master" may be adjusted for process methods and the artwork conductor width may differ from the design width.

2. Design width of conductor is most often stated as a minimum as measured at the base of the conductor. For impedance controlled circuits, a ± tolerance may be placed on conductor width.

**Production Master:** A 1:1 scale pattern which is used to produce one or more printed boards within the accuracy specified on the procurement documentation.

Etch Factor: The ratio of the depth of etch to the amount of lateral etch.

### 3.2.1 Etching Characteristics

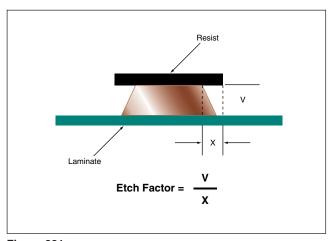


Figure 321a

"A" Point of Narrowest Conductor Width: This is not "Minimum Conductor Width" noted on procurement documentation or performance specifications.

"B" Conductor Base Width: The width that is measured when "Minimum Conductor Width" is noted on the procurement documentation or performance specification.

"C" Production Master Width: This width usually determines the width of the metal or organic resist on the etched conduc-

Design width of the conductor is specified on the procurement documentation and is most often measured at the conductor base "B" for compliance to "Minimum Conductor Width" requirements.

The following two configurations show that conductor width may be greater at the surface than at the base:

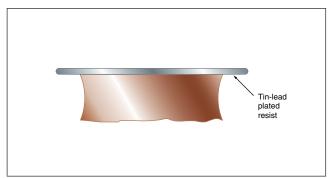
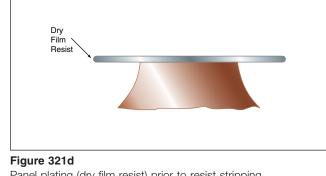


Figure 321b Pattern plating (dry film resist) prior to reflow



Panel plating (dry film resist) prior to resist stripping

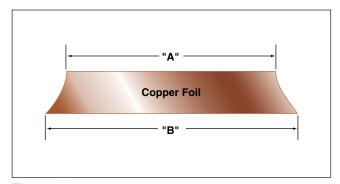


Figure 321c Internal layer after etch

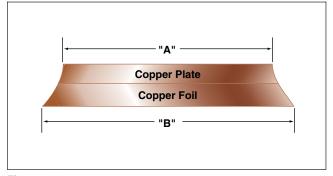


Figure 321e Internal plated layer as used for buried vias

## 3.2.1 Etching Characteristics (cont.)

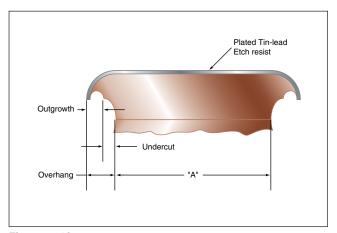


Figure 321f
Pattern plating (dry film resist) with outgrowth

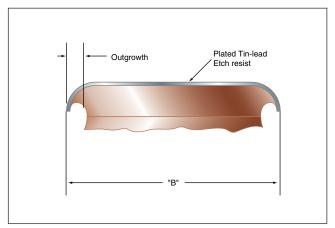


Figure 321h
Pattern plating (liquid resist) with outgrowth

**Note:** The extent of outgrowth, if present, is related to the dry film resist thickness. Outgrowth occurs when the plating thickness exceeds the resist thickness.

Note: The different etch configurations may not meet intended design requirements.

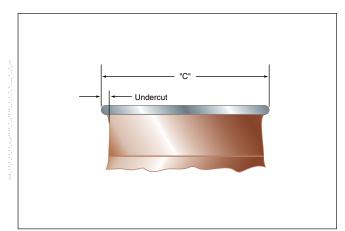
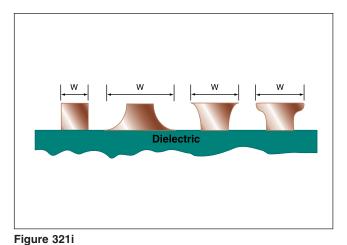


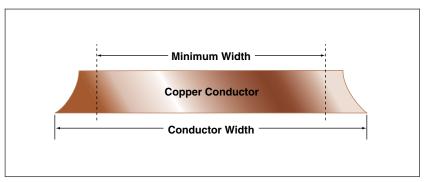
Figure 321g
Thin clad & pattern plating (etch resist)



The effective width of a conductor may vary from the conductor width from surface obstructions (W).

### 3.2.2 Print and Etch

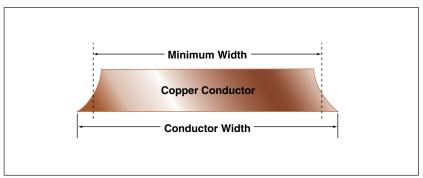
The copper conductor may consist of combinations of copper foil, copper plating and electroless copper. Metal resist, solder coatings, and reflowed tin-lead plating that would normally be seen in a microsection are not shown in these illustrations.



#### Target Condition - Class 1, 2, 3

• Conductor width exceeds minimum requirement.

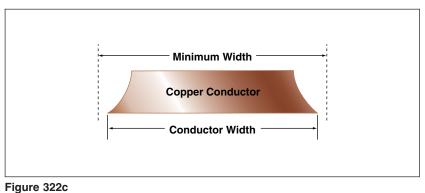
Figure 322a



#### Acceptable - Class 1, 2, 3

• Conductor width meets minimum requirement.

Figure 322b



#### Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

#### 3.2 CONDUCTIVE PATTERNS - GENERAL

### 3.2.3 Surface Conductor Thickness (Foil Plus Plating)

Unless otherwise specified on the procurement documentation, the minimum total (copper foil plus copper plating) conductor thickness after processing **shall** be in accordance with Table 3-1.

Table 3-1 External Conductor Thickness after Plating

	Absolute Cu Min. (IPC-4562 less 10% reduction)	Plus minimum plating for Class 1 and 2	Plus minimum	Maximum Variable Processing Allowance Reduction <sup>3</sup> (μm) [μin]	Minimum Surface Conductor Thickness after Processing (μm) [μin]	
Weight <sup>1,4</sup>	(µm) [µin]	(20 µm) [787 µin] <sup>2</sup>	(25 µm) [984 µin] <sup>2</sup>		Class 1 & 2	Class 3
1/8 oz.	4.60 [181]	24.60 [967]	29.60 [1,165]	1.50 [59]	23.1 [909]	28.1 [1,106]
1/4 oz.	7.70 [303]	27.70 [1,091]	32.70 [1,287]	1.50 [59]	26.2 [1,031]	31.2 [1,228]
3/8 oz.	10.80 [425]	30.80 [1,213]	35.80 [1,409]	1.50 [59]	29.3 [1,154]	34.3 [1,350]
1/2 oz.	15.40 [606]	35.40 [1,394]	40.40 [1,591]	2.00 [79]	33.4 [1,315]	38.4 [1,512]
1 oz.	30.90 [1,217]	50.90 [2,004]	55.90 [2,201]	3.00 [118]	47.9 [1,886]	52.9 [2,083]
2 oz.	61.70 [2,429]	81.70 [3,217]	86.70 [3,413]	3.00 [118]	78.7 [3,098]	83.7 [3,295]
3 oz.	92.60 [3,646]	112.60 [4,433]	117.60 [4,630]	4.00 [157]	108.6 [4,276]	113.6 [4,472]
4 oz.	123.50 [4,862]	143.50 [5,650]	148.50 [5,846]	4.00 [157]	139.5 [5,492]	144.5 [5,689]

Note 1. Starting foil weight of design requirement per procurement documentation.

Note 3. Reference: Min. Cu Plating Thickness

Class 1 = 20  $\mu$ m [787  $\mu$ in] Class 2 = 20  $\mu$ m [787  $\mu$ in] Class 3 = 25  $\mu$ m [984  $\mu$ in]

Note 4. For copper foil above 4 oz., utilize the formula provided below.

The minimum surface conductor thickness after processing values given in Table 3-1 are determined by the following equation:

Minimum Surface Conductor Thickness = a + b - c

#### Where:

- a = Absolute copper foil minimum (IPC-4562 nominal less 10% reduction).
- b = Minimum copper plating thickness (20 µm [787 µin] for Class 1 and Class 2; 25 µm [984 µin] for Class 3).
- c = A maximum variable processing allowance reduction.

Note 2. Process allowance reduction does not allow for rework processes for weights below ½ oz. For ½ oz. and above, the process allowance reduction allows for one rework process.

#### 3.2 CONDUCTIVE PATTERNS - GENERAL

### 3.2.4 Foil Thickness - Internal Layers

Minimum foil thickness (or conductor thickness) is the maximum continuous coplanar thickness that will conduct electrical current.

Individual scratches are included, but the saw-toothed shaped "dendritic" surface for metal-clad adhesion promotion is excluded from the minimum foil thickness determination, as shown in Figure 324a.

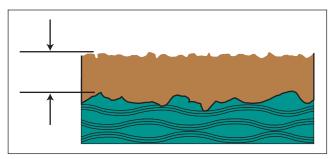


Figure 324a

The minimum internal layer foil thickness after processing shall be in accordance with Table 3-2.

Table 3-2 Internal Layer Foil Thickness after Processing

Weight	Absolute Cu Min. (IPC-4562 less 10% reduction) (µm) [µin]	Maximum Variable Processing Allowance Reduction¹ (μm) [μin]	Minimum Final Finish after Processing (µm) [µin]
1/8 oz. [5.10]	4.60 [181]	1.50 [59]	3.1 [122]
1/4 oz. [8.50]	7.70 [303]	1.50 [59]	6.2 [244]
3/8 oz. [12.00]	10.80 [425]	1.50 [59]	9.3 [366]
1/2 oz. [17.10]	15.40 [606]	4.00 [157]	11.4 [449]
1 oz. [34.30]	30.90 [1,217]	6.00 [236]	24.9 [980]
2 oz. [68.60]	61.70 [2,429]	6.00 [236]	55.7 [2,193]
3 oz. [102.90]	92.60 [3,646]	6.00 [236]	86.6 [3,409]
4 oz. [137.20]	123.50 [4,862]	6.00 [236]	117.5 [4,626]
Above 4 oz. [137.20]	IPC-4562 value less 10% reduction	6.00 [236]	6 μm [236 μin] below minimum thickness of calculated 10% reduction of foil thickness in IPC-4562

Note 1. Process allowance reduction does not allow for rework processes for weights below ½ oz. For ½ oz. and above, the process allowance reduction allows for one rework process.

Note 2. Additional platings that may be required for internal layer conductors shall be separately designated as a plating thickness requirement.

#### 3.3 PLATED-THROUGH HOLES - GENERAL

### Introduction

This section identifies the acceptability characteristics in PTHs used in double-sided and multilayer rigid printed boards. Included in this section are photographic and illustrative depictions of PTH characteristics for both drilled and punched holes, with separate examples where appropriate.

The test specimen **shall** be a representative coupon such as described in IPC-2221, a portion of the printed board being tested, or a whole printed board if within size limits.

Sample holes should be selected at random. Vertical microsections, both parallel and perpendicular to a printed board edge, are recommended. Horizontal microsectioning techniques may be used as the referee. Precise encapsulation and metallurgical techniques **shall** be used to assure highly polished sections with correct part alignment and polishing to the mean of the hole diameter. The polished surface should be etched after initial smear evaluation and just prior to plating thickness measurements.

The evaluation of all properties and requirements **shall** be performed on the thermally stressed test coupon and all requirements **shall** be met. The coupons **shall** be tested after the printed board is exposed to all coating, final finish and thermal processing.

#### **Methods of Inspection:**

- Hole Size (method optional IPC-TM-650, Method 2.2.7)
  - A. Optical
  - B. Document drill blank plug or plug gages
  - C. Tapered hole gage

Note: Hole gages must be cleaned and storage oil must be removed prior to use.

- · Visual hole wall quality
  - A. Voids, nodules, etc., locate with unaided eye, use up to 10X magnification for verification.
  - **B.** Discolorations, stains, etc., use unaided eye and/or solderability tests.

### **Introduction (cont.)**

#### **Microsection:**

#### • Plating thickness measurements

- **A.** Encapsulated Microsection Examination (IPC-TM-650, Method 2.1.1 or Method 2.1.1.2): The average copper thickness should be determined from three measurements, approximately equally spaced, on each side of the PTH. Do not measure in areas having isolated imperfections such as voids, cracks or nodules. Small localized areas with plating thickness less than minimum requirement are evaluated as voids.
- **B.** Nondestructive Method: Micro-ohm Measurements (IPC-TM-650, Method 2.2.13.1): This technique may be used to measure the average copper thickness in PTH when properly standardized. The method has application to measurement of the minimum copper thickness. Due to the dependence on uniform hole geometry this method may not be appropriate for measurement of punched PTHs. The nondestructive feature and the speed and ease of measurement make this method useful in providing variable data for statistical process control.
- C. Plating Thickness: Minimum requirements are established in IPC-6010 series.

#### Solderability

A lot sample or representative specimen should be subjected to a solderability test utilizing Methods B, B1, C, C1, D or D1 of IPC-J-STD-003. The coating durability requirement should be pre-established. The PTHs should exhibit good wetting and capillary action.

### 3.3.1 Annular Ring - Internal Layers

For multilayer printed boards, in addition to physical measurements of printed board surfaces, if internal annular ring breakout is detected in the vertical cross section, but the degree of breakout cannot be determined, internal registration may be assessed by nondestructive techniques other than microsection, such as, special patterns, probes, and/or software, which are configured to provide information on the interpolated annual ring remaining and pattern skew. Techniques include, but are not limited to the following:

- The optional F or R coupon detailed in IPC-2221.
- Custom designed electrically testable coupons.
- Radiographic (x-ray) techniques.
- Horizontal microsection.
- CAD/CAM data analysis as correlated to pattern skew by layer.

**Note:** Microsectioning or statistical sampling **shall** be used to verify correlation of the approved technique, and a calibration standard established for the specific technique employed.

If misregistration to the point of breakout is detected in vertical microsections, the concerns are that:

- 1. The conductor width minimum may be compromised at the land junction and,
- 2. There is insufficient electrical spacing.

The extent and direction of breakout **shall** be determined. Appropriate test coupons or actual production printed boards **shall** be tested at the affected area(s) and analyzed on the suspect layer(s) to determine compliance. This may be accomplished by the techniques listed above.

Measurements for internal annular ring are taken at the copper hole wall plating/internal land interface to the outer most tip of the internal land as shown in Figure 331a.

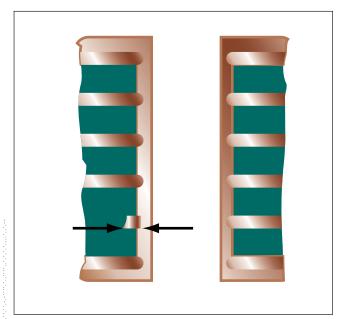


Figure 331a

### 3.3.1 Annular Ring - Internal Layers (cont.)

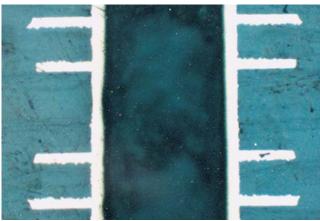


Figure 331b

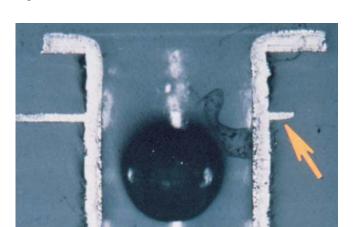


Figure 331c

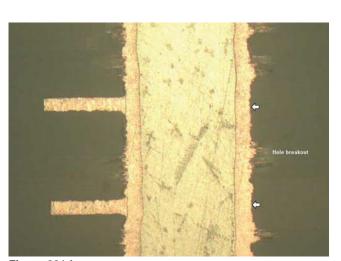


Figure 331d

#### Target Condition - Class 1, 2, 3

• All holes accurately registered in the center of the lands.

#### Acceptable - Class 3

• Annular ring measures 0.025 mm [0.000984 in] or more.

#### Acceptable - Class 2

 90° hole breakout is allowed provided the land/conductor junction is not reduced below the allowable width reduction in 2.10.1.1 and minimum lateral spacing is maintained.

#### Acceptable - Class 1

• Hole breakout is allowed provided the land/conductor junction is not reduced below the allowable width reduction in 2.10.1.1 and minimum lateral spacing is maintained.

#### Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

#### 3.3 PLATED-THROUGH HOLES - GENERAL

# 3.3.2 Lifted Lands - (Cross-Sections)

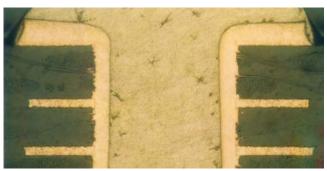


Figure 332a

### Target Condition - Class 1, 2, 3

• No lifting of lands.

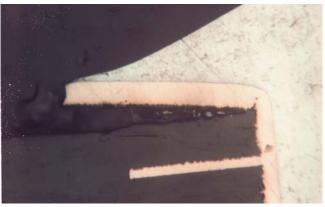


Figure 332b

### Acceptable - Class 1, 2, 3

After thermal stress testing or rework simulation:

• Lifted lands are allowed.

# 3.3.3 Foil Crack - (Internal Foil) "C" Crack

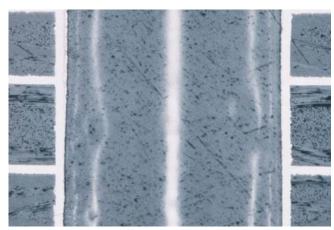


Figure 333a

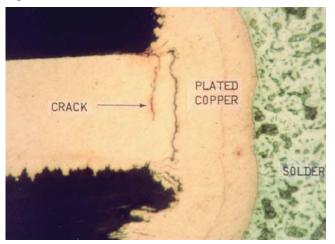


Figure 333b

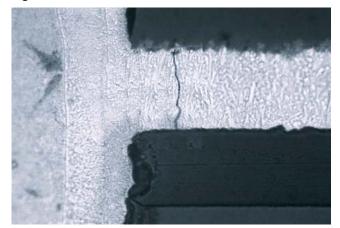


Figure 333c

### Target Condition - Class 1, 2, 3

• No cracks in foil.

#### Acceptable - Class 2, 3

• No evidence of cracks in foil.

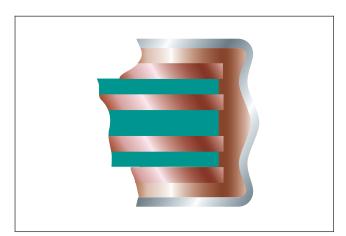
#### Acceptable - Class 1

• Allowed on one side of hole only and does not extend through foil thickness.

#### Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

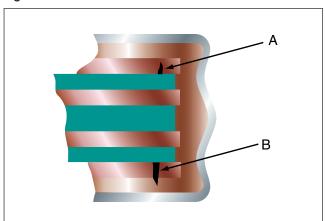
### 3.3.4 Foil Crack (External Foil)



Target Condition - Class 1, 2, 3

• No cracks in foil.

Figure 334a



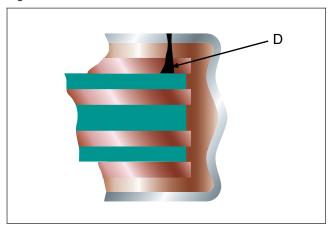
Acceptable - Class 1, 2, 3

• Crack A

### Acceptable - Class 1

• Cracks B

Figure 334b



Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria

Figure 334c

Note: "A" Crack is a crack in external foil.

"B" Crack is a crack that does not completely break plating (minimum plating remains).

"D" Crack is a complete crack through external foil and plating.

# 3.3.5 Plating Crack (Barrel) "E" Crack

Target Condition - Class 1, 2, 3Barrel plating is free of cracks.

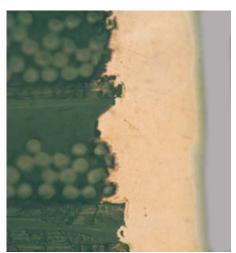


Figure 335a

## Acceptable - Class 1, 2, 3

• No cracks in plating.



Figure 335b



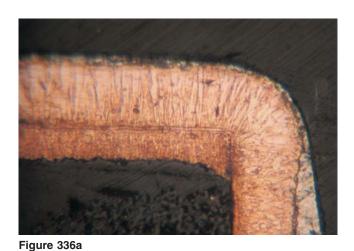
Figure 335c

### Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

#### 3.3 PLATED-THROUGH HOLES - GENERAL

## 3.3.6 Plating Crack - (Corner) "F" Crack



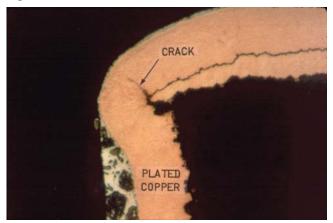


Figure 336b

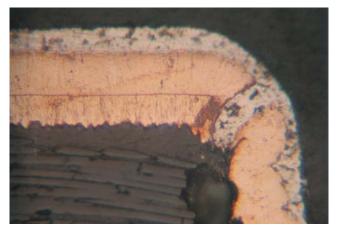


Figure 336c

### Target Condition - Class 1, 2, 3

• No cracks in plating.

#### Acceptable - Class 1, 2, 3

• No cracks in plating.

#### Nonconforming - Class 1, 2, 3

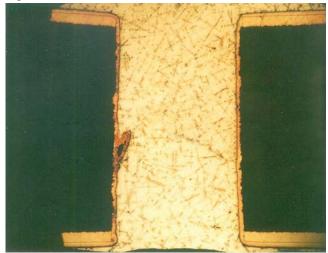
• Defects either do not meet or exceed above criteria.

### 3.3.7 Plating Nodules

## Target Condition - Class 1, 2, 3

• Plating is smooth and uniform throughout the hole. No evidence of roughness or nodules.

Figure 337a



#### Acceptable - Class 1, 2, 3

• Roughness or nodules do not reduce plating thickness below absolute minimum requirements or hole diameter below minimum requirements.

Figure 337b



Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

•

### 3.3.8 Copper Plating Thickness - Hole Wall

The average copper thickness should be determined from three measurements, approximately equally spaced, on each side of the PTH. Do not measure in areas having isolated imperfections such as voids, cracks or nodules.

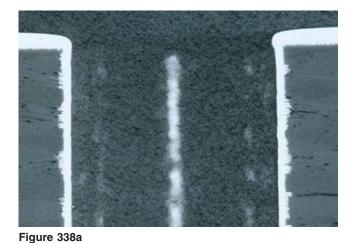




Figure 338b

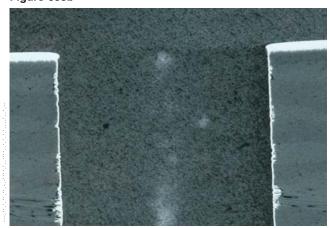


Figure 338c

#### Target Condition - Class 1, 2, 3

• Plating is smooth and uniform throughout the hole. Plating thickness meets requirements.

### Acceptable - Class 1, 2, 3

- Plating thickness varies but meets minimum average requirements and minimum thin area requirements in the IPC-6010 series.
- Small localized areas with plating thickness less than minimum requirement are evaluated as voids.

#### Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

### 3.3.9 Copper Wrap Plating

Copper wrap plating minimum as specified in the IPC-6010 series **shall** be continuous from the filled plated hole onto the external surface of any plated structure and extend by a minimum of 25 µm [984 µin] where an annular ring is required as shown in Figure 339a.

Reduction of surface wrap copper plating by processing (sanding, etching, planarization, etc.) resulting in insufficient wrap plating is not allowed as shown in Figure 339b.

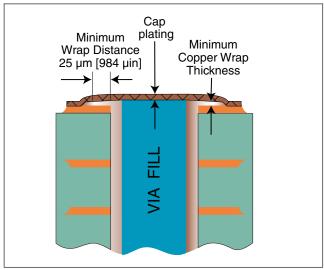


Figure 339a Surface Copper Wrap Measurement (Applicable to all filled PTHs)

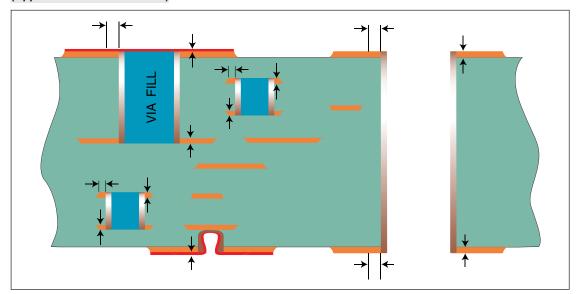


Figure 339b Wrap Copper Removed by Excessive Sanding/Planarization (Not Acceptable)

Note: Dimension lines and arrows indicate where wrap copper has been removed.

Note: Cap plating, if required, over filled holes is not considered in wrap copper thickness measurements.

# 3.3.9 Copper Wrap Plating (cont.)

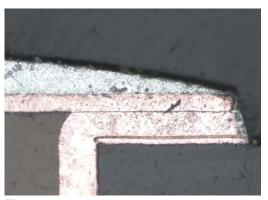


Figure 339c

# Target Condition - Class 1, 2, 3 Acceptable - Class 3

- Wrap plating is continuous from the filled plated hole onto the external surface and extends by a minimum of 25 µm [984 µin] where an annular ring is required.
- Wrap thickness is not less than 12 µm [472 µin] for through, blind and buried vias ≥ two layers..
- Wrap thickness is not less than 6 µm [236 µin] for blind and buried microvias.
- $\bullet$  Wrap thickness is not less than 7  $\mu m$  [276  $\mu in$ ] for buried via cores (two layers).
- Reduction of surface wrap copper plating by processing (sanding, etching, planarization, etc.) does not result in insufficient wrap plating.



Figure 339d

Laminate craci

Figure 339e

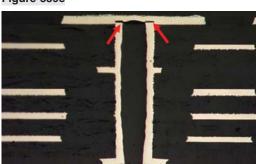


Figure 339f

# Acceptable - Class 1, 2

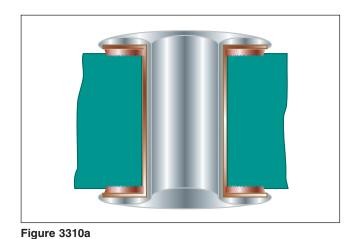
- Wrap plating is continuous from the filled plated hole onto the external surface.
- Wrap thickness is not less than 5 μm [197 μin] for all through-hole and via structures.
- Reduction of surface wrap copper plating by processing (sanding, etching, planarization, etc.) does not result in insufficient wrap plating.

# Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

Note: Cap plating, if required, over filled holes is not considered in wrap copper thickness measurements.

# 3.3.10 Plating Voids



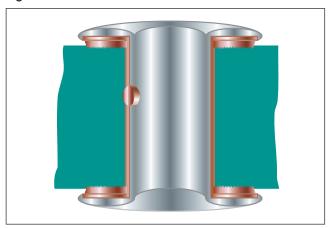


Figure 3310b

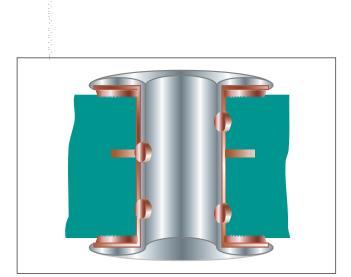


Figure 3310c

Visual observations made on cross-sections only.

# Target Condition - Class 1, 2, 3

• Hole is free of voids.

# Acceptable - Class 2, 3

- No more than one plating void per test coupon or production printed board, regardless of length or size.
- No plating void in excess of 5% of the total printed board thickness.
- No plating voids evident at the interface of an internal conductive layer and plated hole wall.
- Plating voids less than or equal to 90° of the circumference.

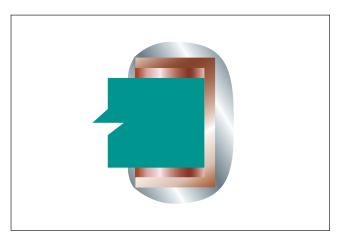
# Acceptable - Class 1

- No more than three plating void per test coupon or production printed board, regardless of length or size.
- No plating void in excess of 5% of the total printed board thickness.
- No plating voids evident at the interface of an internal conductive layer and plated hole wall.
- Plating voids less than or equal to 90° of the circumference.

# Nonconforming - Class 1, 2, 3

# 3.3.11 Solder Coating Thickness (Only When Specified)

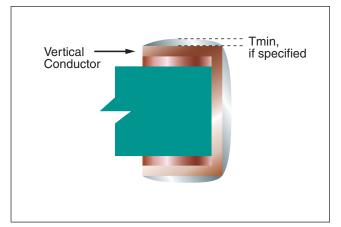
Solder coating thickness, when specified, shall be evaluated prior to thermal stress.



# Target Condition - Class 1, 2, 3

• Solder coating thickness is uniform and covers etched land edge. Exposed copper is not evident.

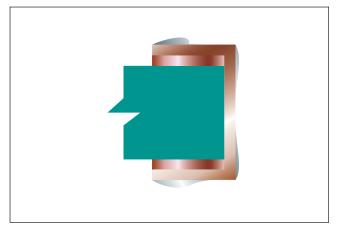
Figure 3311a



# Acceptable - Class 1, 2, 3

 Solder coating thickness is uniform. Vertical (conductor and land) areas may not be covered. No exposed copper is evident.

Figure 3311b



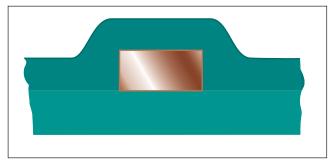
Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

Figure 3311c

Note: For solderability requirements, see 5.1.

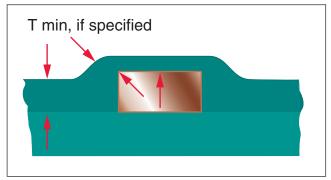
# 3.3.12 Solder Mask Thickness



# Target Condition - Class 1, 2, 3

• Thickness as specified on procurement documentation.

Figure 3312a



Acceptable - Class 1, 2, 3

• Specified: The solder mask thickness meets the thickness requirements on the procurement documentation (cannot be visually assessed).

Figure 3312b

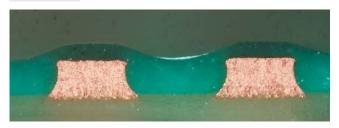


Figure 3312c

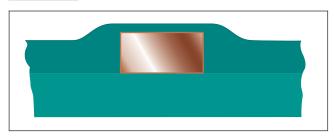


Figure 3312d

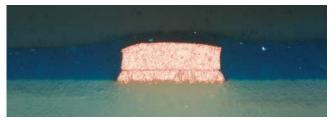


Figure 3312e

# Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

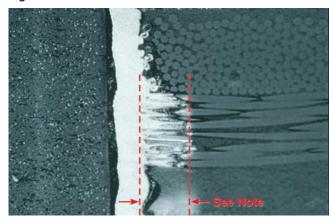
# **3.3.13 Wicking**



Target Condition - Class 1, 2, 3

• No wicking present.

Figure 3313a



Acceptable - Class 3

• Wicking does not exceed 80 µm [3,150 µin].

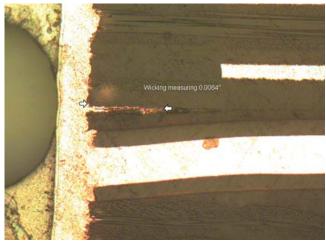
### Acceptable - Class 2

• Wicking does not exceed 100 µm [3,937 µin].

# Acceptable - Class 1

• Wicking does not exceed 125 µm [4,921 µin].

Figure 3313b



Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

Figure 3313c

Note: Wicking is measured from the laminate edge excluding the plating.

# 3.3.13.1 Wicking, Clearance Holes

# D

# Figure 33131a

- A) Surface Pad B) Dielectric
- C) Adjacent Noncommon Conductors
- D) Surface Plating

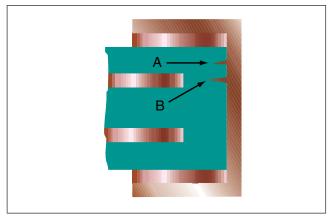


Figure 33131b

# Acceptable - Class 3

Target Condition - Class 1, 2, 3

along the reinforcement material.

- Wicking (A) does not exceed 80 µm [3,150 µin]
- Wicking (B) does not reduce conductor spacing less than specified minimum on the procurement documentation.

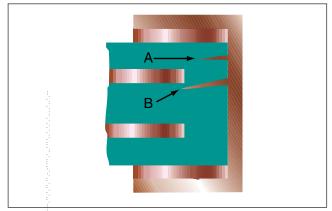
· No wicking of conductive material into base material or

# Acceptable - Class 2

- Wicking (A) does not exceed 100 µm [3,937 µin]
- Wicking (B) does not reduce conductor spacing less than specified minimum on the procurement documentation.

# Acceptable - Class 1

- Wicking (A) does not exceed 125 µm [4,921 µin]
- Wicking (B) does not reduce conductor spacing less than specified minimum on the procurement documentation.



Visual observations made on cross-sections only.

Figure 33131c

# Nonconforming - Class 1, 2, 3

# 3.3.14 Innerlayer Separation - Vertical (Axial) Microsection

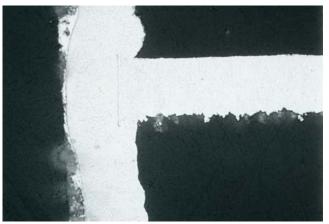


Figure 3314a

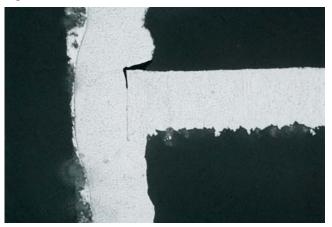


Figure 3314b

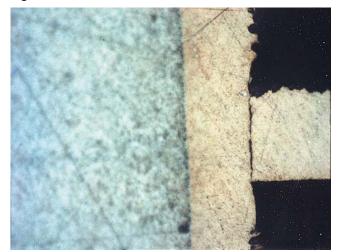


Figure 3314c

# Target Condition - Class 1, 2, 3

 Direct bond of plated copper to copper foil. No evidence of innerlayer separation (separation between internal lands and plating of the hole wall) or innerlayer inclusions.

# Acceptable - Class 2, 3

• No separation evident.

# Acceptable - Class 1

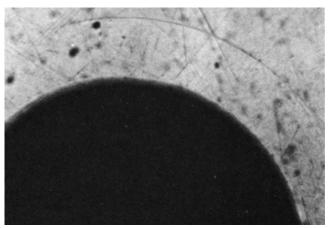
• Partial innerlayer separation or innerlayer inclusions on only one side of hole wall at each land location on no more than 20% of each available land.

# Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

# 3.3 PLATED-THROUGH HOLES - GENERAL

# 3.3.15 Innerlayer Separation - Horizontal (Transverse) Microsection



# Figure 3315a

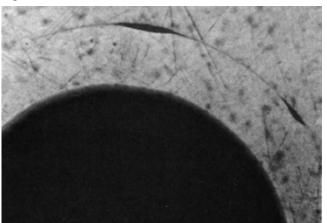


Figure 3315b

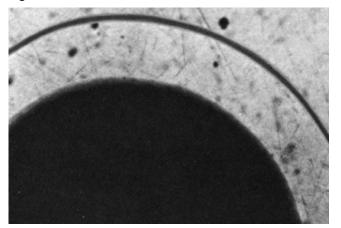


Figure 3315c

# Target Condition - Class 1, 2, 3

 No separation between the internal layer and plating in the hole. Direct bond of plated copper to layer foil copper. Line of demarcation caused by preferential etching of electroless copper deposit.

# Acceptable - Class 2, 3

• No separation evident.

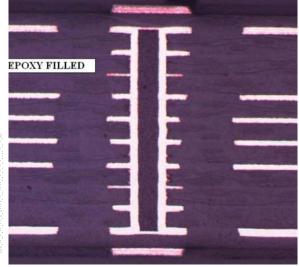
# Acceptable - Class 1

• Slight line of demarcation and localized minor innerlayer separation that does not exceed specified requirements.

# Nonconforming - Class 1, 2, 3

# 3.3.16 Material Fill of Blind and Buried Vias

Blind via holes should be filled or plugged with a polymer or solder mask to prevent solder from entering them as solder in the small holes tends to decrease reliability. Incomplete via fill may result in printed board delamination due to the rapid expansion of entrapped air pockets or flux contaminants during solder reflow processes. Requirements for buried via fill are listed below.



# Target - Class 1, 2, 3

• Complete fill of blind or buried via with laminating resin or similar fill material.



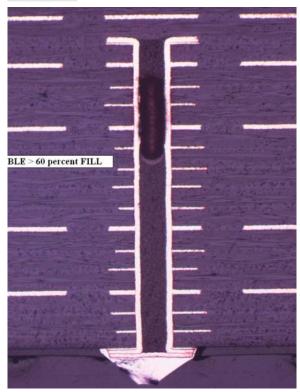


Figure 3316b

Note: Through hole fill requirements are AABUS.

Acceptable - Class 1, 2, 3

• At least 60% buried via fill with laminating resin or similar fill material.

# Acceptable - Class 2, 3

• At least 60% fill for blind vias with an aspect ratio greater than 1:1 or as specified in the procurement documentation.

# 3.3 PLATED-THROUGH HOLES - GENERAL

# 3.3.16 Material Fill of Blind and Buried Vias (cont.)

# Acceptable - Class 1

• Buried vias completely void of fill material.

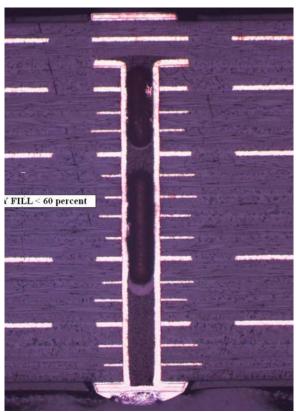


Figure 3316c

# Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

Note: Through hole fill requirements are AABUS.

# 3.3.17 Cap Plating of Filled Holes

When copper cap plating of filled holes is specified by the master drawing the following shall apply.

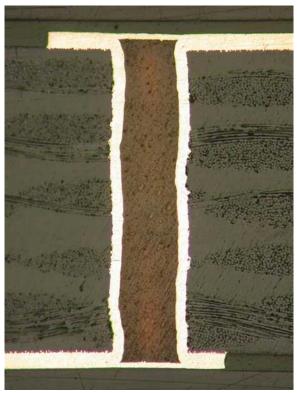


Figure 3317a

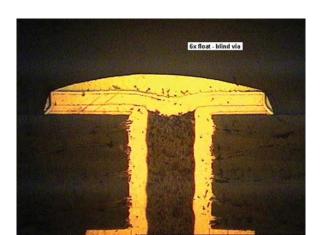


Figure 3317b

# Target Condition - Class 1, 2, 3

• Copper surface is planar with no protrusion (bump) and/or depression (dimple)

# Acceptable - Class 1, 2, 3

- Separation of copper cap to fill material.
- No separation of the cap plating to underlying plating.
- Cap protrusion (bump) and/or depression (dimple) meets the dimensional requirements in IPC-6012.
- Fill material within the blind via **shall** be planar with the surface within ± 0.076 mm [0.003 in] unless otherwise specified.
- When cap plating is specified, fill material within the blind via shall meet the dimple/bump requirements of IPC-6012.
- No voids in the cap plating over the resin fill.

# 3.3 PLATED-THROUGH HOLES - GENERAL

# 3.3.17 Cap Plating of Filled Holes (cont.)

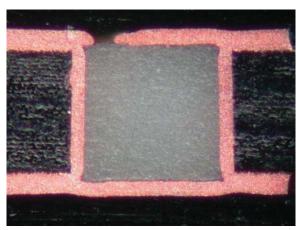


Figure 3317c

# Nonconforming - Class 1, 2, 3

### 3.4 PLATED-THROUGH HOLES - DRILLED

# Introduction

This section identifies the acceptability characteristics for drilled PTHs. Although only two characteristics are identified (burrs and nailheading), good drilling is essential for a good PTH. The drilled hole wall should be smooth and free of burrs, delamination, burning, crushed insulation, and protruding fibers. The hole should be perpendicular, round and not tapered. A poorly drilled hole may cause other problems that have been described and characterized in other sections of this document. These problems are:

- Rough plating
- Nodules
- Plating voids
- Thin plating
- Plating cracks (hole wall, corner)
- Wicking (excessive)
- Hole size reduction
- Pink ring
- Blow holes in soldering
- Skip plating

The physical appearance of a particular hole will be affected by one or more of the following variables:

- Drill point angle
- Drill rotation speed
- Drill feed rate
- Drill sharpness

Nailheading is a condition which may develop during the drilling operation. Worn drills, improper speeds and feeds, and/or soft back up and entry materials usually cause nailheading. The condition is acceptable for all classes.

# 3.4 PLATED-THROUGH HOLES - DRILLED

# 3.4.1 Burrs



Figure 341a

# Target Condition - Class 1, 2, 3

• No evidence of burrs.

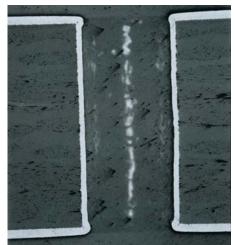


Figure 341b

# Acceptable - Class 1, 2, 3

• Burrs are acceptable for all classes provided they do not reduce hole diameter or plating thickness below required minimums.

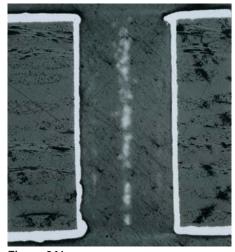


Figure 341c

# Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

# 3.4 PLATED-THROUGH HOLES - DRILLED

# 3.4.2 Nailheading

No evidence exists that nail heading affects functionality. The presence of nail heading may be considered an indicator of process or design variation but is not a cause for rejection. Consider evaluation for glass bundle damage.

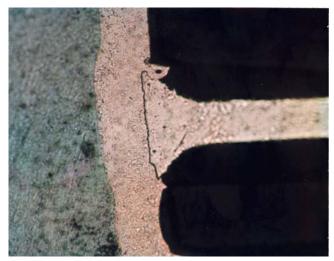


Figure 342a

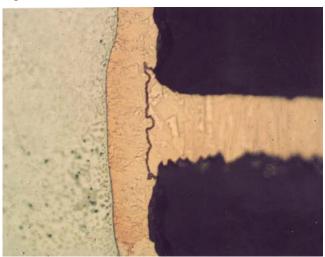


Figure 342b

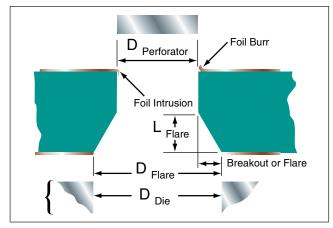
### 3.5 PLATED-THROUGH HOLES - PUNCHED

# Introduction

The figures below depict a punched hole and a punched and plated hole in a reinforced laminate. The figures show the characteristics which may be exhibited in a punched hole. Punched holes may appear different than drilled holes. Drilled holes have straight wall geometry while the geometry of punched holes will vary from straight to those seen in the figures. The difference in the hole characteristics are attributed to:

- Laminate type and thickness
- Thickness and type of cladding
- Design of punch and die
- Tool maintenance
- Processing techniques

The laminate type is very important in determining its punchability. Laminates in which all the base material is woven fabric are difficult to punch. The composite materials utilizing a woven fabric top and bottom sheet and a random fiber internal mat are easily punched and the straight wall geometry of the drilled hole can be approached. Punch and die clearance and sharpness are also important when a straight wall is desired and a small flare is required. The amount of flare, foil burr, foil intrusion, laminate bulge, and laminate rollover seen in the figures do not necessarily degrade the plated-through hole quality and are acceptable for all classes provided other requirements are in compliance with the performance specifications and the engineering description.



Copper Cladding

Laminate Bulge Plating

Cladding

Laminate Rollover

t

Fiber

Metallic Overplate

Annular Ring

Figure 35a Punched

Figure 35b Punched and Plated

Although burrs and fibers can also be associated with the straight wall geometry of a drilled hole, the concepts of flare and intrusion relate specifically to punched hole formation techniques. An intrusion of copper foil within the punched hole can result from excessive punch-to-die clearance or a dull punch. Tapered flare or breakout is a normal condition on the exit side of a punched hole and may be caused by the stress generated within the laminate during hole formation. The degree of flare can be controlled through variations in punch-to-die clearance and other operating parameters.

# 3.5.1 Roughness and Nodules

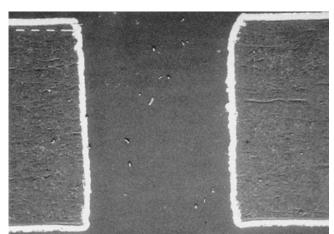


Figure 351a

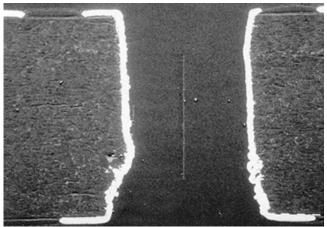


Figure 351b

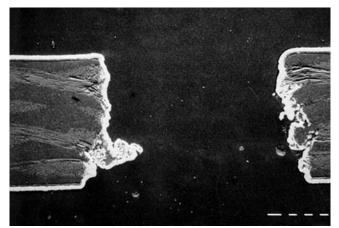


Figure 351c

# Target Condition - Class 1, 2, 3

• Plating is smooth and uniform throughout the hole. No evidence of roughness or nodules.

# Acceptable - Class 1, 2, 3

• Roughness or nodules do not reduce plating thickness or hole diameter below minimum requirements.

# Nonconforming - Class 1, 2, 3

# 3.5 PLATED-THROUGH HOLES - PUNCHED

# 3.5.2 Flare

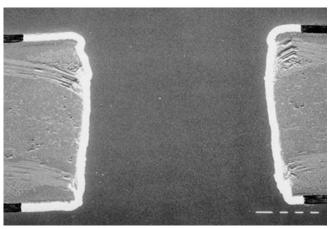


Figure 352a

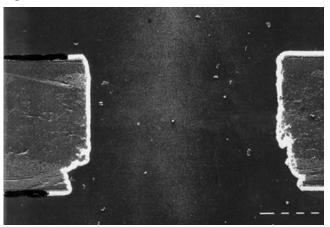


Figure 352b

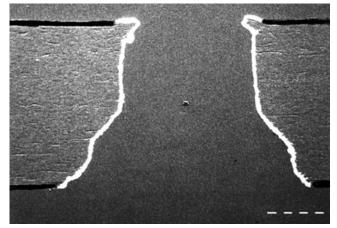


Figure 352c

# Target Condition - Class 1, 2, 3

• Hole exhibits only slight flare and does not violate minimum annular ring requirements.

# Acceptable - Class 1, 2, 3

• Hole exhibits flare but it does not violate minimum annular ring requirements.

# Nonconforming - Class 1, 2, 3

# **4 MISCELLANEOUS**

# Introduction

This section provides acceptability criteria for several special printed board types. The distinctive features of these special printed board types require supplementing the general acceptability criteria. For each special printed board type, this section outlines where and how the general acceptability criteria are supplemented. The special printed board types are:

- Flexible
- Rigid-Flex
- Metal Core
- Flush

# Introduction

This section covers the acceptability requirements specific to flexible and rigid-flex printed boards. Parameters not covered in this section are to be evaluated using the other sections of this document.

The numeric type designator for flexible and rigid-flex printed boards differs from that of rigid printed boards. The various types for flexible and rigid-flex printed boards are defined as follows:

- Type 1 Single-sided flexible printed boards containing one conductive layer, with or without stiffeners.
- Type 2 Double-sided flexible printed boards containing two conductive layers with PTHs, with or without stiffeners.
- Type 3 Multilayer flexible printed board containing three or more conductive layers with PTHs, with or without stiffeners.
- Type 4 Multilayer rigid and flexible material combinations containing three or more layers with PTHs.
- Type 5 Flexible or rigid-flex printed boards containing two or more conductive layers without PTHs.

The types referred to in this section on flexible and rigid-flex printed boards will use the definitions above.

The physical requirements for folding flexibility and flexibility endurance are not described in this document. If required by the procurement documentation, refer to IPC-6013 for details.

# 4.1.1 Coverlay Coverage - Coverfilm Separations

Imperfections such as wrinkles, creases, and nonlamination are acceptable provided they do not exceed the limits for foreign inclusions in 2.3.4 and the limits below.

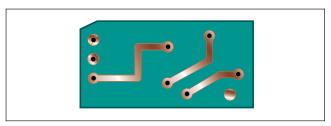


Figure 411a

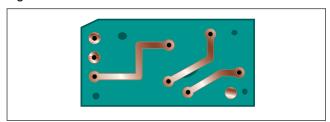


Figure 411b

# Target Condition - Class 1, 2, 3

- Uniform and no separations or delamination.
- No wrinkles, creases or soda strawing.

# Acceptable - Class 1, 2, 3

Delamination and nonlamination meets the following criteria:

- At random locations away from conductors, each separation is no larger than 0.80 x 0.80 mm [0.0315 x 0.0315 in] and is not within 1.0 mm [0.0394 in] of the printed board edge or the coverfilm opening.
- The total number of separations does not exceed three in any 25 x 25 mm [0.984 x 0.984 in] of coverfilm surface area.
- The total separation does not exceed 25% of the spacing between adjacent conductors.
- No coverfilm nonlamination along the outer edges of the coverfilm

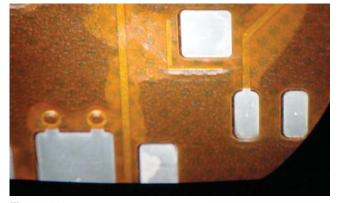


Figure 411c

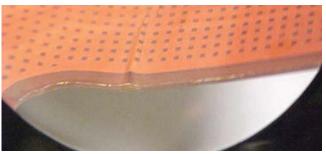


Figure 411d

# Nonconforming - Class 1, 2, 3

# 4.1.2 Coverlay/Covercoat Coverage - Adhesives

The covercoat coverage **shall** have the same requirements as the solder mask coatings in the rigid printed board section of this document. This section covers the acceptability requirements for coverlay coverage including squeeze-out of adhesive over the solderable land area and foil surface.

# 4.1.2.1 Adhesive Squeeze-Out - Land Area

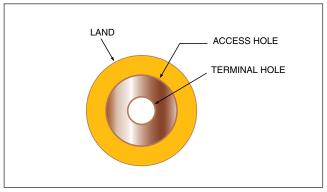


Figure 4121a

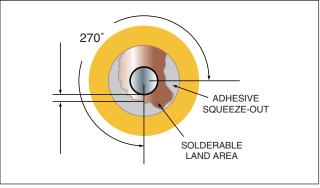


Figure 4121b

# Target Condition - Class 1, 2, 3

• No unwanted material on land area.

# Acceptable - Class 3

• A 0.05 mm [0.00197 in] solderable annular ring for 360° of the circumference.

### Acceptable - Class 2

• A 0.05 mm [0.00197 in] solderable annular ring for at least 270° of the circumference.

# Acceptable - Class 1

A solderable annular ring for at least 270° of the circumference.

# Nonconforming - Class 1, 2, 3

# 4.1.2.2 Adhesive Squeeze-Out - Foil Surface

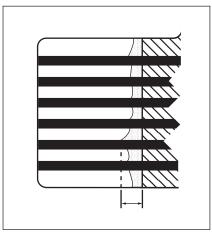


Figure 4122a

# Target Condition - Class 1, 2, 3

• No unwanted material on foil surface.

# Acceptable - Class 3 70 µm foil and below:

• ≤0.2 mm [0.0079 in].

# Above 70 µm foil

• ≤0.4 mm [0.0157 in] or AABUS.

# Acceptable - Class 1, 2 70 µm foil and below:

• ≤0.3 mm [0.0118 in]

# Above 70 µm foil

• ≤0.5 mm [0.0197 in] or AABUS.



Figure 4122b

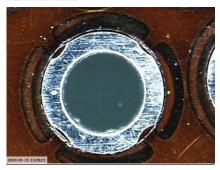


Figure 4122c

# Nonconforming - Class 1, 2, 3

# 4.1.3 Access Hole Registration for Coverlay and Stiffeners

In cases where anchoring spurs are attached to the lands, they shall be lapped by the coverlay.

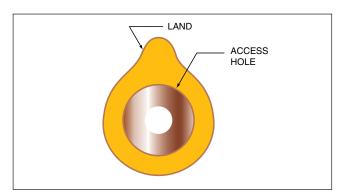


Figure 413a

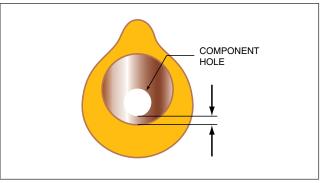


Figure 413b

### Target Condition - Class 1, 2, 3

• Meets nominal registration.

### Acceptable - Class 3

- Coverlay or stiffener does not extend into the hole.
- For supported holes, a solderable annular ring of 0.05 mm [0.00197 in] or more for the full circumference.
- For unsupported holes, a solderable annular ring of 0.25 mm [0.00984 in].

### Acceptable - Class 2

- Coverlay or stiffener does not extend into the hole.
- A solderable annular ring for 270° or more of the circumference.

# Acceptable - Class 1

- Coverlay or stiffener does not extend into the hole.
- A solderable annular ring for 180° or more of the circumference.

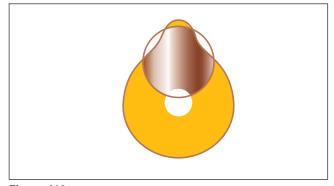


Figure 413c

# Nonconforming - Class 1, 2, 3

# 4.1.4 Plating Defects

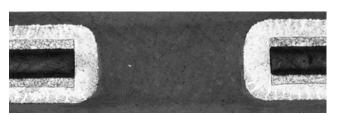


Figure 414a

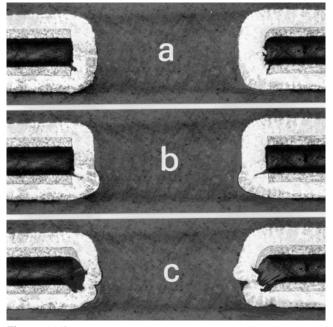


Figure 414b

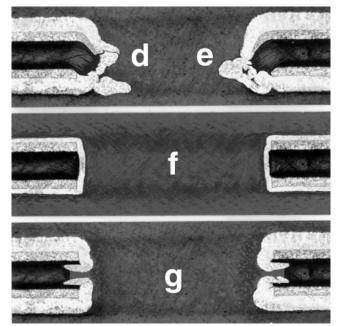


Figure 414c

# Target Condition - Class 1, 2, 3

- Plating is uniform and meets the minimum thickness requirements.
- No defects of the plating or base material present.

# Acceptable - Class 1, 2, 3

- Minor defects present but meet the minimum requirements:
  - a. Slight deformation of base material and minor smear.
  - b. Adhesive or dielectric filament with small nodule, but copper thickness meets minimum requirements.
  - c. Localized thin and non-uniform plating; copper slightly thin over one corner and minor extrusion of base material, but copper thickness meets minimum requirements.

### Nonconforming - Class 1, 2, 3

- Defects either do not meet or exceed above criteria and/or the following:
- d. Adhesive filament causing cracks in plating.
- e. Nodules, extrusion and deformation of base material violate minimum hole size requirements.
- f. Plating violates the minimum thickness requirement.
- g. Circumferential voids.

# 4.1.5 Stiffener Bonding

The stiffener is evaluated for mechanical support only by way of the test method listed below.

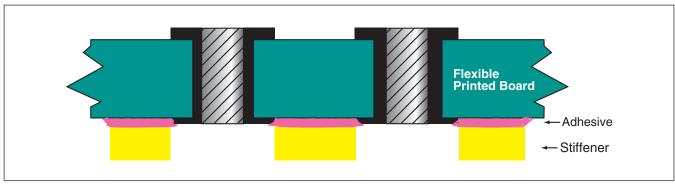


Figure 415a

### Acceptable - Class 1, 2, 3 (Stiffener)

- Mechanical support is required; void-free bonding is not required.
- The stiffener does not reduce the solderable annular ring below the minimum solderable annular ring requirements.
- Peel strength between the flexible printed board and the stiffener, when tested in accordance with the method below, is a minimum of 1.4kg per 25 mm [0.984 in] width when bonded with thermoset adhesive and 0.38kg per 25 mm [0.984 in] width when bonded with pressure sensitive adhesive.

### Acceptable - Class 3 (Adhesive)

- The adhesive used to bond the stiffener does not reduce the solderable annular ring below the minimum solderable annular ring requirements.
- The total area of voids does not exceed 10% of the stiffener surface area.
- Each void does not exceed 2.5 mm [0.0984 in] in the longest dimension.

# Acceptable - Class 2 (Adhesive)

- The adhesive used to bond the stiffener does not reduce the solderable annular ring below the minimum solderable annular ring requirements.
- The total area of voids does not exceed 20% of the stiffener surface area.
- Each void does not exceed 2.5 mm [0.0984 in] in the longest dimension.

# Acceptable - Class 1 (Adhesive)

- The adhesive used to bond the stiffener does not reduce the solderable annular ring below the minimum solderable annular ring requirements.
- The total area of voids does not exceed 30% of the stiffener surface area.
- Each void does not exceed 2.5 mm [0.0984 in] in the longest dimension.

### Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

**Test Method:** Using a sharp instrument such as a scalpel or razor blade, cut approximately 10 mm [0.394 in] wide by 80 mm [3.15 in] long through the flexible printed board to the stiffener so that approximately halfway through the peeling operation the sample will be perpendicular to the pull. Pull at a rate of  $50 \pm 6.3$  mm/minute. Take readings at the beginning, middle, and end of the pull, and average the reading for acceptability.

# 4.1.6 Transition Zone, Rigid Area to Flexible Area

The transition zone is the area centered at the edge of the rigid portion from which the flexible portion extends. The inspection range is limited to 3.0 mm [0.12 in], about the center of the transition, which is the edge of the rigid portion.

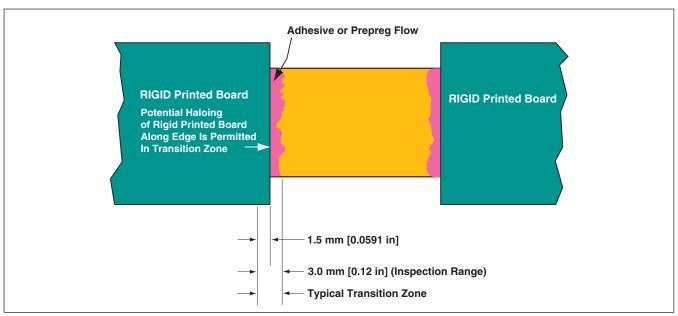


Figure 416a

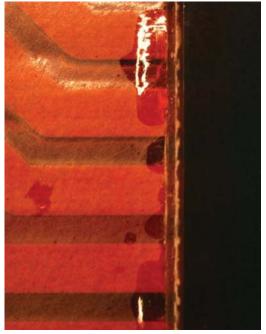


Figure 416b

# Acceptable - Class 1, 2, 3

- Adhesive squeeze-out.
- Localized deformation of dielectric or conductors.
- Protruding dielectric material.

# Nonconforming - Class 1, 2, 3

# 4.1.7 Solder Wicking/Plating Penetration Under Coverlay

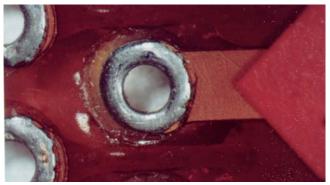


Figure 417a

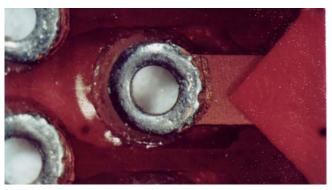


Figure 417b

### Target Condition - Class 1, 2, 3

- Solder or plating on land covers all exposed metal and stops at coverlay.
- Solder wicking or plating penetration does not extend into the bend or flex transition area.

# Acceptable - Class 3

- Solder wicking/plating penetration does not extend under coverlay more than 0.1 mm [0.004 in].
- Solder wicking or plating penetration does not extend into the bend or flex transition area.
- Meets conductor spacing requirements.

# Acceptable - Class 2

- Solder wicking/plating penetration does not extend under coverlay more than 0.3 mm [0.012 in].
- Solder wicking or plating penetration does not extend into the bend or flex transition area.
- Meets conductor spacing requirements.



Figure 417c

# Acceptable - Class 1

- Solder wicking/plating penetration does not extend under coverlay more than 0.5 mm [0.020 in].
- Solder wicking or plating penetration does not extend into the bend or flex transition area.
- Meets conductor spacing requirements.

# Nonconforming - Class 1, 2, 3

# 4.1.8 Laminate Integrity

This section shows the voids and cracks that may be present in flexible or rigid-flex printed boards. The requirements for the flexible portion differ from the rigid-flex portion and are defined in the text even though only a rigid-flex section is shown.

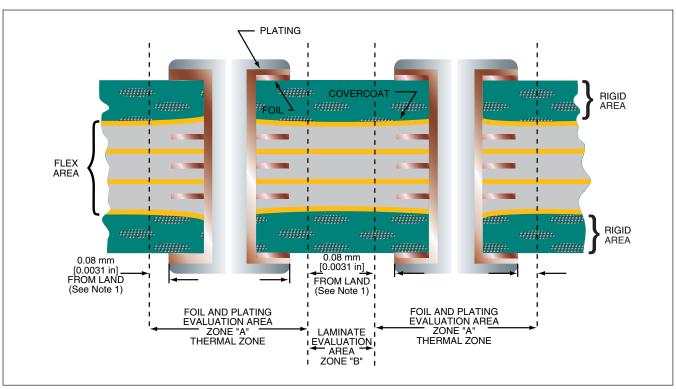


Figure 418a

# Notes:

- 1. The thermal zone extends 0.08 mm [0.0031 in] beyond the end of the land that is most radially extended.
- 2. Laminate anomalies or imperfections in Zone A areas are not evaluated on specimens, which have been exposed to thermal stress or rework simulation.
- 3. Multiple voids or cracks between PTHs in the flex area and in the same plane shall not have combined length exceeding the limit.

### **Target Condition**

• No laminate voids or cracks.

# 4.1.8.1 Laminate Integrity - Flexible Printed Board

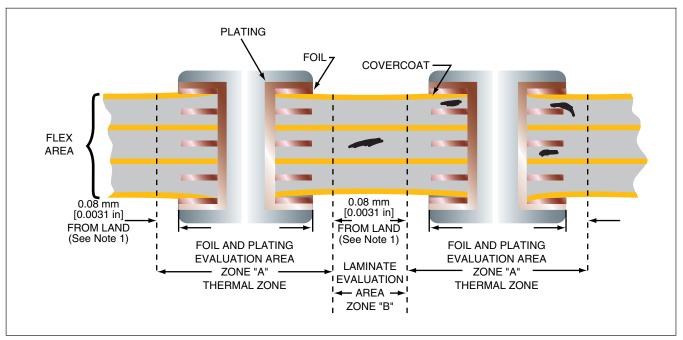


Figure 4181a

### Notes:

- 1. The thermal zone extends 0.08 mm [0.0031in] beyond the end of the land that is most radially extended.
- 2. Multiple voids or cracks between PTHs and in the same plane shall not have combined length exceeding the limits for all classes.

# **Target Condition**

• No laminate voids or cracks.

# Acceptable - Class 1, 2, 3

- Laminate voids or cracks are not evaluated in Zone A.
- Laminate voids or cracks in the flexible printed board do not exceed 0.50 mm [0.020 in] in Zone B.

# Nonconforming - Class 1, 2, 3

# 4.1.8.2 Laminate Integrity - Rigid-Flex Printed Board

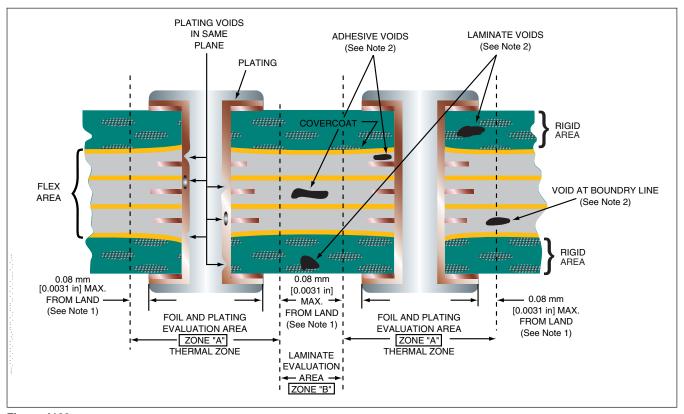


Figure 4182a

### Notes:

- 1. The thermal zone extends 0.08 mm [0.0031 in] beyond the end of the land that is most radially extended.
- 2. Multiple voids or cracks between PTHs in the flex area and in the same plane **shall not** have combined length exceeding the limits for all classes.

### **Target Condition**

• No laminate or adhesive voids or cracks.

# Acceptable - Class 2, 3

- Laminate voids or cracks are not evaluated in Zone A.
- Laminate voids or cracks that originate in Zone A and extend into Zone B or are entirely in Zone B, in the rigid portion of the printed board, are not in excess of 0.08 mm [0.0031 in] in Zone B.
- Adhesive voids or cracks that originate in Zone A and extend into Zone B or are entirely in Zone B, in the flexible portion of the
  printed board, are not in excess of 0.5 mm [0.020 in] in Zone B.

# Acceptable - Class 1

- Laminate voids or cracks are not evaluated in Zone A.
- Laminate voids or cracks that originate in Zone A and extend into Zone B or are entirely in Zone B, in the rigid portion of the printed board, are not in excess of 0.15 mm [0.00591 in] in Zone B.
- Adhesive voids or cracks that originate in Zone A and extend into Zone B or are entirely in Zone B, in the flexible portion of the printed board, are not in excess of 0.5 mm [0.020 in] in Zone B.

# Nonconforming - Class 1, 2, 3

# 4.1.9 Etchback (Type 3 and Type 4 Only)

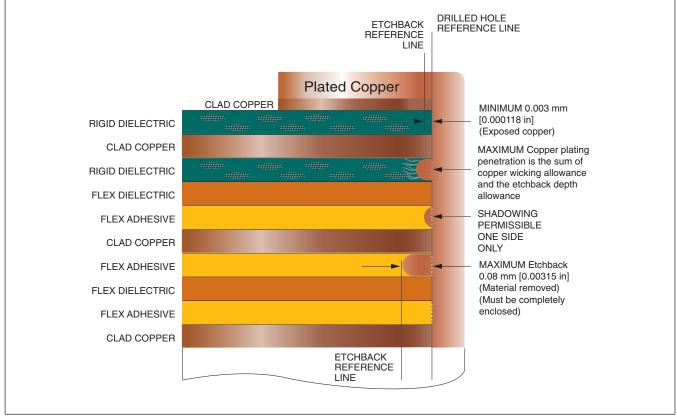


Figure 419a

**Note:** Due to various materials used in the construction of rigid-flex printed boards, varying degrees of preferential etchback are exhibited among the various materials.

### Target Condition/Acceptable - Class 1, 2, 3

- Etchback between 0.003 and 0.08 mm [0.00012 and 0.0031 in].
- Shadowing permitted on one side of each land.

### Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

**Caution:** Etchback greater than 0.05 mm [0.0020 in] may cause folds or voids in the plating, which then may not meet the required copper thickness.

# 4.1.10 Smear Removal (Type 3 and 4 Only)

Smear removal is the removal of debris that results from the formation of the hole. Smear removal should be sufficient to completely remove resin from the surface of conductor interface.

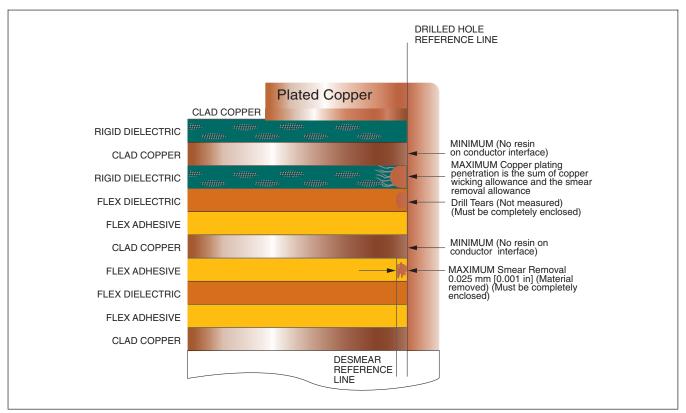


Figure 4110a

Note: Smear removal is not required of Type 1 or Type 2 flexible printed boards.

# Target Condition/Acceptable - Class 1, 2, 3

- Smear removal process not etched back more than 0.025 mm [0.001 in].
- Random tears or gouges that produce small areas where the 0.025 mm [0.001 in] depth is exceeded, provided dielectric spacing is maintained.

# Nonconforming - Class 1, 2, 3

# 4.1.11 Trimmed Edges/Edge Delamination



Figure 4111a

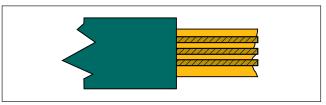


Figure 4111b



Figure 4111c

# Target Condition - Class 1, 2, 3

- Free of nicks and tears. Minimum edge to conductor spacing maintained.
- The trimmed edge of the flexible printed board or the flexible section of the finished rigid-flex printed board is free of burrs, nicks, delamination, and tears.

# Acceptable - Class 1, 2, 3

- No nicks, burrs or delamination in excess of that specified in the procurement documentation.
- No tears in Type 1 or Type 2 flexible printed boards.
- No tears in the flexible portion of Type 3 or Type 4 flexible printed boards.
- Nicks and tears that occur as a result of tie-in tabs to facilitate circuit removal as AABUS.
- Edge to conductor spacing of the flexible portion is within requirements specified on the procurement documentation.
- Nicks or haloing along the printed board edges, cutouts, and unsupported holes of the rigid portion of a rigid/flex printed board, providing the penetration does not exceed 50% of the distance from the edge to the nearest conductor or more than 2.5 mm [0.0984in], whichever is less.

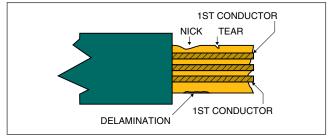


Figure 4111d

# Acceptable - AABUS

 When nicks and tears occur as a result of tie-in tabs to facilitate circuit removal, the extent of these imperfections does not exceed the requirements agreed to by user and supplier.

# 4.1.11 Trimmed Edges/Edge Delamination (cont.)



Figure 4111e

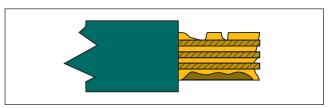


Figure 4111f

# Nonconforming - Class 1, 2, 3

# 4.1.12 Fold/Bend Marks

A fold mark is characterized by bending in a sharp angle as shown in Figure 4112a. A bend mark is characterized by a bend whose radius is an obtuse angle, as shown in Figure 4112b.

# Target Condition - Class 1, 2, 3

• Free of voids, scratches or foreign material.



Figure 4112a

# Acceptable - Class 1, 2, 3

- The fold mark meets the requirements of 4.1.1 for coverlay coverage.
- No fold marks along the conductor pattern.
- No cracks or opening of the conductor pattern.
- Bending marks.

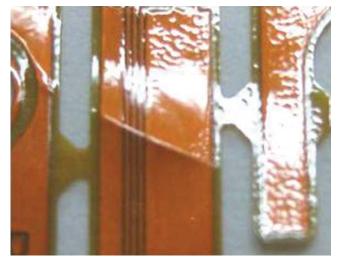


Figure 4112b

# Nonconforming - Class 1, 2, 3

#### 4.1 FLEXIBLE AND RIGID-FLEX PRINTED BOARDS

# 4.1.13 Silver Film Integrity

Silver film can be used for electro-static discharge (ESD) shielding in flexible printed boards. Scratches and voids may occur on the surface of the silver film when the liner material is peeled away.

#### Target Condition - Class 1, 2, 3

• Free of voids, scratches or foreign material.

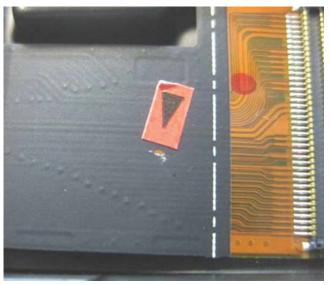


Figure 4113a



Figure 4113b

#### Acceptable - Class 1, 2, 3

- Voids, scratches or foreign material do not exceed 5 locations per side.
- Voids, scratches or foreign material do not expose metal underneath the silver film (exposed coverlay underneath is acceptable).
- Voids are less than 3.0 x 3.0 mm [0.118 x 0.118 in] in size.
- The width of scratches does not exceed 1.5 mm [0.060 in], and their length does not exceed 50% of the length of the flexible printed board.
- Touch up by black oil pen (see Figure 4113c).

#### 4.1 FLEXIBLE AND RIGID-FLEX PRINTED BOARDS

# 4.1.13 Silver Film Integrity (cont.)

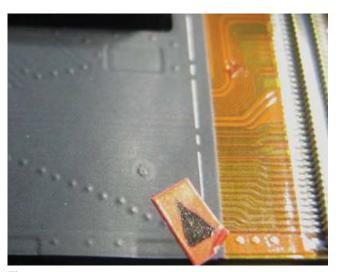


Figure 4113c

#### Nonconforming - Class 1, 2, 3

#### Introduction

There are two types of metal core printed boards, both having one or more conductive patterns on each side of an insulated metal substrate. Interconnection between conductive patterns is made with PTHs.

In the first type, for double-sided printed boards, the metal core is laminated on each side with single-sided copper clad laminate to form a two-sided printed board with the conductors subsequently etched and plated by conventional printed board processes. For multilayer applications, additional etched internal layers may be laminated to the core or multiple cores. The cores may serve as a heat sink, a power or ground plane, or as a constraining plane to decrease the coefficient of thermal expansion (CTE) of the printed board in the planar direction.

For this type, the cores are commonly aluminum, copper, or (for CTE control) copper clad invar or molybdenum. If the cores are not to be electrically connected to the circuitry (as is normally the case with aluminum cores), clearance holes for PTHs are drilled or punched prior to lamination and filled with an insulating material. Copper cores may be electrically connected through the PTH. However, copper clad invar or molybdenum requires special processing to make acceptable electrical connections.

In the second type of metal core printed board, clearance holes are drilled, punched or machined in the bare core and it is then coated with an insulating material by spray coating, electrophoretic processes, or fluidized bed techniques. The coating must be pinhole free and of the specified thickness required to withstand electrical leakage and arc-over. After coating, the insulation is covered with electroless copper and plated and etched to provide required surface conductors and PTHs. For this type, the core may be copper, aluminum or steel, and most often acts as a heat sink or stiffener.

#### 4.2.1 Type Classifications

#### **Metal Core Printed Board Types**

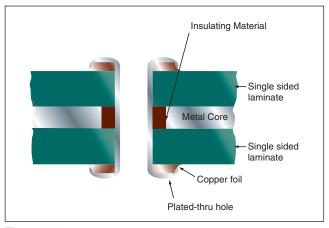


Figure 421a

#### **Laminated Type Metal Core Printed Board**

 Single conductive layer on both sides and insulated from the metal core substrate. Conductive material to be copper foil and electrodeposited copper.

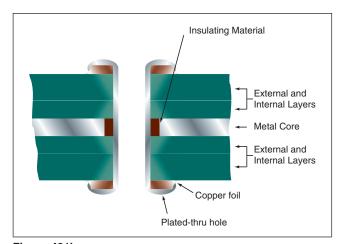


Figure 421b

#### **Laminated Type Metal Core Multilayer Printed Board**

 More than one conductive layer on one or both sides and insulated from the metal core substrate. Conductive material to be copper foil and electrodeposited copper.

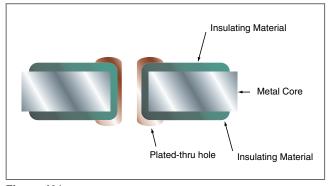


Figure 421c

#### **Insulated-Metal-Substrate Metal Core Printed Board**

 Single conductive layer on both sides and insulated from the metal core substrate. Conductive material to be electroless copper and a copper flash is then applied over all surfaces.
 From this point on, document printed board fabrication processes are employed. This process is generally limited to double-sided printed boards only.

## 4.2.2 Spacing Laminated Type

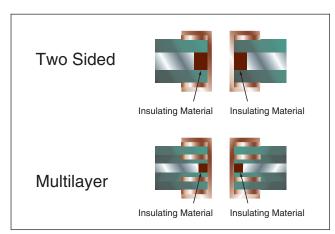
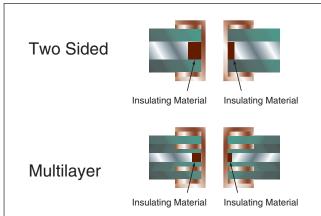


Figure 422a

Figure 422b

# Target Condition - Class 1, 2, 3

• The spacing between the metal core and adjacent conductive surfaces exceeds 0.1 mm [0.0040 in].



Two Sided Insulating Material Insulating Material Multilayer Insulating Material Insulating Material

Figure 422c

#### Acceptable - Class 1, 2, 3

• The spacing between the metal core and the PTH or the metal core and adjacent conductive surfaces is greater than 0.1 mm [0.0040 in].

#### Nonconforming - Class 1, 2, 3

## 4.2.3 Insulation Thickness, Insulated Metal Substrate

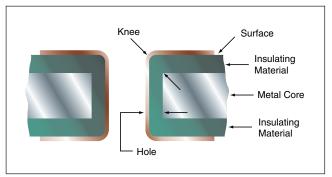


Figure 423a

# Acceptable - Class 1, 2, 3

Target Condition - Class 1, 2, 3

• Insulation thickness meets requirements of the table below.

• Insulation thickness exceeds requirements of the table

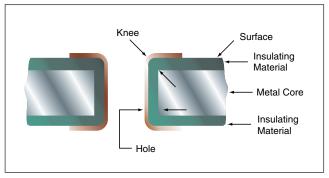


Figure 423b

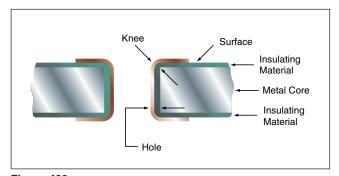


Figure 423c

#### Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

	Insulation Process*			
Description	Α	В	С	D
Hole (minimum)	0.050 mm [0.0020 in]	0.025 mm [0.000984 in] - 0.065 mm [0.00256 in]	0.125 mm [0.004921 in]	0.125 mm [0.004921 in]
Surface (minimum)	0.050 mm [0.0020 in]	0.025 mm [0.000984 in] - 0.065 mm [0.00256 in]	0.125 mm [0.004921 in]	N/A
Knee** (minimum)	0.025 mm [0.000984 in]	0.025 mm [0.000984 in]	0.075 mm [0.00295 in]	N/A

<sup>\*</sup>Applies to insulated-metal-substrate board only.

Process A - Spray Coating

Process B - Electrophoretic Deposition

Process C – Fluidized Bed Process

Process D - Molding Process

<sup>\*\*</sup>Junction where the hole wall and surface meet.

#### 4.2.4 Insulation Material Fill, Laminated Type Metal Core

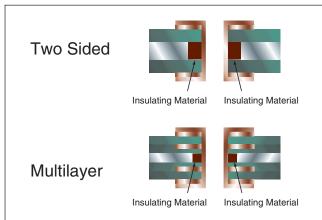


Figure 424a

#### Target Condition - Class 1, 2, 3

 Insulation material fills the entire area between the PTH and the metal core without any voids or areas of missing insulation.

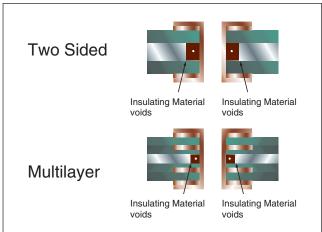


Figure 424b

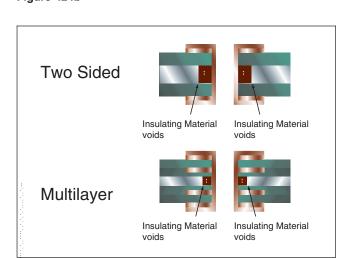


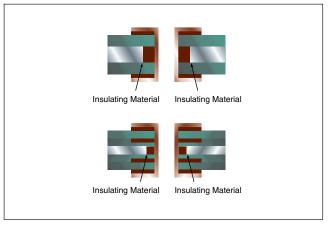
Figure 424c

#### Acceptable - Class 1, 2, 3

- Insulating material meets minimum thickness and dielectric spacing requirements.
- Voids or resin recession does not cause spacing to be less than acceptability requirements.

#### Nonconforming - Class 1, 2, 3

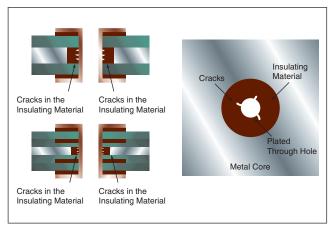
## 4.2.5 Cracks in Insulation Material Fill, Laminated Type



Target Condition - Class 1, 2, 3

• There are no cracks in the insulating fill material.

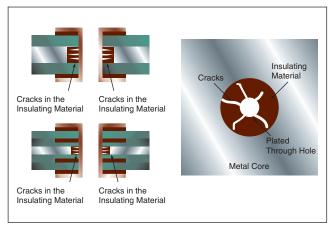
Figure 425a



#### Acceptable - Class 1, 2, 3

- Wicking, radial cracks, lateral spacing or voids in the hole-fill insulation material does not reduce the electrical spacing between adjacent conductive surfaces to less than 100 µm [0.003937 in].
- $\bullet$  Wicking and/or radial cracks does not exceed 75  $\mu m$  [0.00295 in] from the PTH edge into the hole-fill.

Figure 425b



Nonconforming - Class 1, 2, 3

Figure 425c

# 4.2.6 Core Bond to Plated-Through Hole Wall

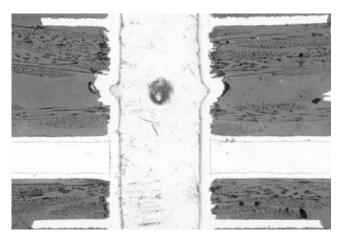
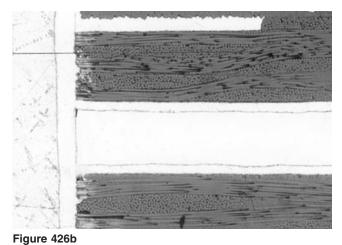


Figure 426a

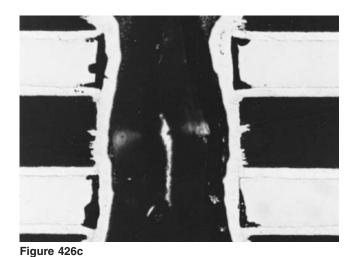
#### Target Condition - Class 1, 2, 3

• Complete bond on both sides.



#### Acceptable - Class 1, 2, 3

Interconnection separation not more than 50% of the non-copper core thickness. If copper clad core is used it **shall not** have any separation in the copper portion of the interconnect.



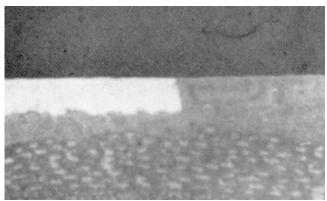
#### Nonconforming - Class 1, 2, 3

#### Introduction

This section covers acceptability criteria for flush printed boards. In flush printed boards, the surfaces, holes and other parameters for acceptability are the same as in standard single-and double-sided printed boards. This section covers the additional parameters that are important to the evaluation of flush printed boards.

#### 4.3.1 Flushness of Surface Conductor

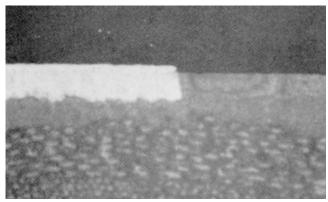
The application of flush circuitry requires that the conductor surfaces and the base material be essentially in the same plane.



Target Condition - Class 1, 2, 3

• Conductor is flush to the base material or surrounding insulating material surface.





Acceptable - Class 1, 2, 3

• Conductor is not flush but meets the minimum requirements.



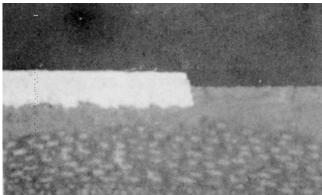


Figure 431c

#### Nonconforming - Class 1, 2, 3

#### **5 CLEANLINESS TESTING**

#### Introduction

The purpose of this section is to assist the reader in better understanding the importance of correct handling procedures in order to avoid damage and contamination during cleanliness testing.

The following general rules minimize surface contaminants when handling printed boards:

- 1. Work stations should be kept clean and neat.
- 2. There should be no eating, drinking or use of tobacco products at the work station or other activities that are likely to cause contamination of the printed board surfaces.
- 3. Hand creams and lotions containing silicone should not be used since they could result in solderability and other processing problems. Specially formulated lotions are available.
- 4. Handling of printed boards by their edges is desirable.
- 5. Lint free cotton or disposable plastic gloves should be used when handling bare printed boards. Gloves should be changed frequently as dirty gloves can cause contamination problems.
- 6 Unless special racks are provided, stacking printed boards without interleaving protection should be avoided. Cleanliness testing is used to determine organic or inorganic, and ionizable or nonionizable contaminants.

The following are examples of the more common contaminants found on printed boards:

- 1. Flux residues
- 2. Particulate matter
- 3. Chemical salt residues
- 4. Fingerprints
- 5. Corrosion (oxides)
- 6. White residues

Due to the destructive nature of contaminants, it is recommended that cleanliness requirements of applicable procurement documentation be adhered to.

The solvent resistivity **shall** be in accordance with IPC-6010 series unless otherwise specified. The specimens **shall** be tested for ionic contamination in accordance with IPC-TM-650, Method 2.3.25 and 2.3.26.

#### **5.1 SOLDERABILITY TESTING**

#### Introduction

This section describes the methods and requirements for solderability testing. Solderability of printed boards verifies the state of the printed board expected during assembly. Solderability testing is performed on both the surface and PTHs. IPC-J-STD-003 describes in detail the different solderability tests as shown in Table 5-1:

Table 5-1 Test Method Selection within IPC-J-STD-003

Test Method	Applies to Surface Features	PTHs		
Tests with Visual Assessment Criteria				
A – Edge Dip Test A1 – Edge Dip Test	X	N/A		
B - Rotary Dip Test B1 - Rotary Dip Test	X (Solder Source Side Only)	Х		
C - Solder Float Test C1 - Solder Float Test	X (Solder Source Side Only)	Х		
D – Wave Solder Test D1 – Wave Solder Test	X (Solder Source Side Only)	Х		
E - Surface Mount Simulation Test E1 - Surface Mount Simulation Test	X	N/A		
Tests with Force Measurement Criteria				
F – Wetting Balance Test F1 – Wetting Balance Test	X	Х		

Along with the solderability method, the user **shall** specify as part of the purchase order agreement, the required coating durability. The following are guidelines for determining the needed level of coating durability, not product performance classes. Durability conditioning and solderability testing **shall** be performed per IPC-J-STD-003.

#### Coating Durability categories:

Category 1 - Minimum Coating Durability; intended for printed boards which will be soldered within 30 days from the time of manufacture and are likely to experience minimum thermal exposures.

Category 2 – Average Coating Durability; intended for printed boards likely to experience storage up to six months from the time of manufacture and moderate thermal or solder exposures.

Category 3 – Maximum Coating Durability; intended for printed boards likely to experience long storage (over six months) from the time of manufacture, and may experience severe thermal or solder processing steps, etc. It should be recognized that there may be a cost premium or delivery delay associated with printed boards ordered to this durability level.

The test specimen **shall** be a representative coupon, a portion of the printed board being tested, or a whole board if within size limits, such that a immersion depth defined in the individual method is possible. Sample holes should be selected at random.

#### 5.1.1 Plated-Through Holes (Applicable to Test C/C1)

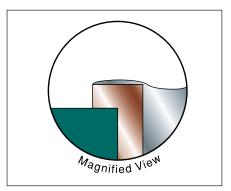


Figure 511a

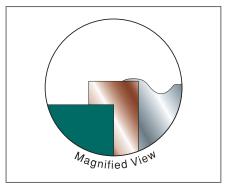






Figure 511d

#### Target Condition - Class 1, 2, 3

- Solder has risen in all plated holes.
- There is no nonwetted or exposed base metal.

#### Acceptable - Class 3

- Solder has risen in all plated holes.
- Solder fully wets the walls of the hole.
   There is no evidence of nonwetting or exposed base metal on any PTH.

#### Acceptable - Class 1, 2

- Solder fully wets the wall area of the PTH holes.
- Solder shall plug 1.5 mm [0.0591 in] diameter (complete filling is not necessary).

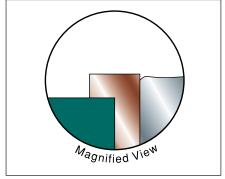


Figure 511c

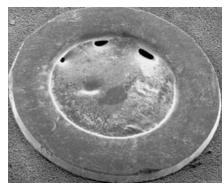


Figure 511e

#### Nonconforming - Class 1, 2, 3

#### **5.2 ELECTRICAL INTEGRITY**

## Introduction

Testing of printed boards shall be in accordance with IPC-9252 unless otherwise AABUS.



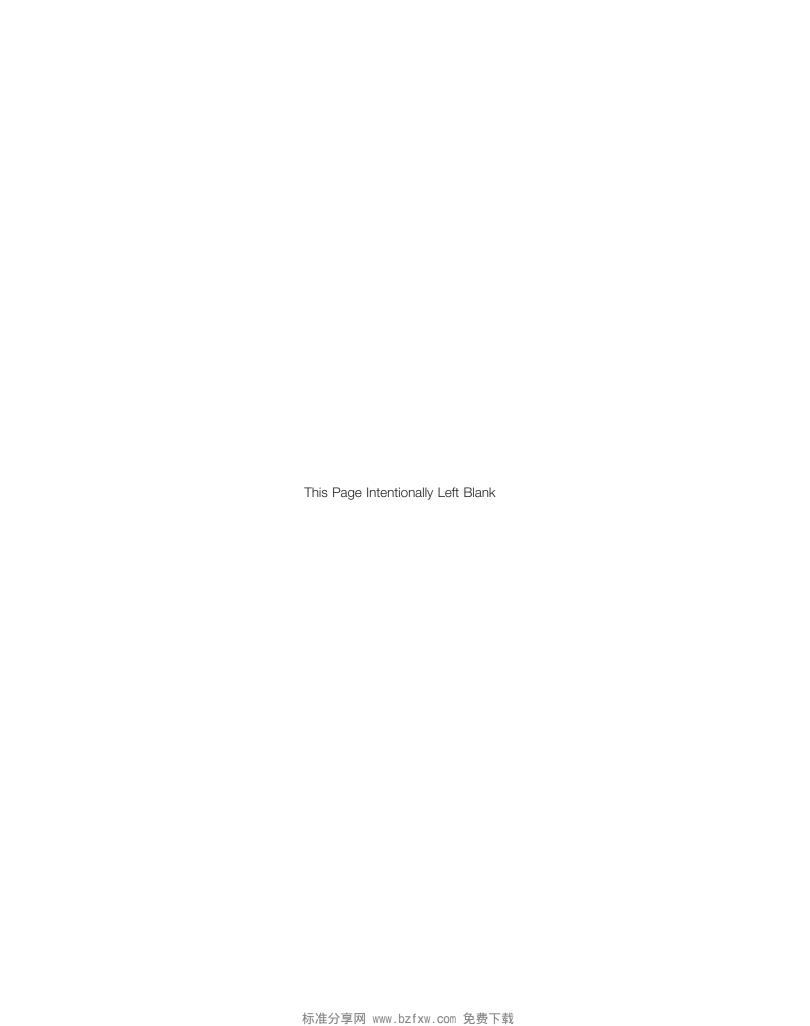
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The purpose of this form is to keep current with terms routinely used in the industry and their definitions. Individuals or companies are invited to comment. Please

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Term		Definition			
		If space not adequate, use reverse side or attach additional sheet(s)			
Artwork: ☐ Not Applicable ☐ Included: Electro	•	e supplied			
Document(s) to which this terr	m applies:				
Committees affected by this te	erm:				
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IPC O		Committee 2-30			
Date Received:		Date of Initial Review:			
Comments Collated:		Comment Resolution:			
Returned for Action:		Committee Action: ☐ Accepted ☐ Rejected			
Revision Inclusion:		Accept Modify			
	IFC	Classification			

# Classification Code • Serial Number Terms and Definition Committee Final Approval Authorization: Committee 2-30 has approved the above term for release in the next revision. IPC 2-30 Committee: Date:





# **Standard Improvement Form**

The purpose of this form is to provide the Technical Committee of IPC with input from the industry regarding usage of the subject standard.

Individuals or companies are invited to submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:			
Requirement, paragraph number			
Test Method number, paragraph number			
The referenced paragraph number has proven to be:			
Unclear Too Rigid In Error			
Other			
2. Recommendations for correction:			
2 01 1 1 1			
3. Other suggestions for document improvement:			
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- Participate in problem-solving exchanges on a vast range of industry-specific issues and concerns through IPC's technical e-mail forums.
- Network with other industry professionals at premier industry events such as the international IPC APEX EXPO as well as the regional IPC Midwest Conference & Exhibition.
- Get priority responses to your technical questions from IPC's technical staff.

# Shape the Industry

**BECOME PART OF** a worldwide network of professionals who are actively involved in shaping the future of our industry.

- Participate in developing industry standards your company, customers, competitors and suppliers use. IPC standards are internationally accepted due to affiliation with the American National Standards Institute (ANSI) and International Electrotechnical Commission (IEC).
- Make your voice heard in the regulations that affect your company by taking advantage of IPC-organized environmental and public policy activities.

# Train Your People

**INCREASE YOUR KNOWLEDGE** and facilitate continuous learning among your technical staff.

- Attend any of the 75-plus workshops and international conferences IPC sponsors annually, where the exchange of technical information is unequalled.
- Participate in IPC's voluntary training and certification programs for a cost-effective, industry-recognized way to demonstrate your commitment to quality.
- Purchase IPC's award-winning CD- and DVD-based training materials at a discount, to cost-effectively build the foundation of your company's training program.

# Market Your Business



USE IPC'S GLOBAL reach and exclusive member benefits to increase your company's visibility.

- Build your brand by using the IPC member logo to highlight your company's involvement, plus get free links from IPC's Web site to your Web site.
- Be listed in IPC's online membership directory available to all IPC members.
- Put your products, services and qualifications in front of key customers with a listing in IPC's Products and Services Index (PCB and EMS companies only).
- Exhibit in IPC's annual trade show and conference, IPC APEX EXPO, plus the IPC Midwest Conference & Exhibition at a special member price.
- Gain valuable exposure by sponsoring market research conferences and Management Meetings at discounted rates.

# Contain Costs

TAKE ADVANTAGE OF exclusive savings opportunities that can easily offset your annual membership investment.

- Get discounts of up to 50 percent on IPC standards, publications and training materials.
- Save money on subscription purchases of IPC standards through IHS. Save up to 25 percent.
- Enjoy dramatic discounts on registration fees for meetings, technical conferences, workshops and tutorials.
- Benefit from preferred pricing on exhibit space at IPC trade shows and events.

# Join the Leaders in IPC

WHATEVER SEGMENT OF the industry you are in — PCB design, board manufacturing, electronics manufacturing services (EMS), original equipment manufacturer (OEM), industry supplier, government agency, educational institution — IPC membership has something to offer virtually everyone at your site. Put the resources of the entire industry behind your company by joining IPC today!

For more than 50 years, company leaders have looked to IPC – Association Connecting Electronics Industries® for the tools, information and forums they need to thrive in the ever-changing electronic interconnect industry.

As a member-driven organization and leading source for industry standards, training, market research and public policy advocacy, IPC supports programs to meet the needs of the estimated \$1.5 trillion (U.S. dollars) global electronics industry.

Whatever your role in the industry — a small start-up company, an educational or government institution or a Fortune® 500 firm — you can join more than 2,700 companies worldwide that enjoy access to unparalleled opportunities to participate in and shape the direction of our collective future.

To learn more about IPC membership and apply online, visit www.ipc.org.



# **Application for Site Membership**

Thank you for your decision to join IPC. Membership is **site specific**, which means that IPC member benefits are available to all individuals employed at the site designated on the next page of this application.

To help IPC serve your member site in the most efficient manner possible, please tell us what your facility does by choosing the most appropriate member category. (Check one box only.)

	Printed Circuit Board Manuf	acturers			
	This facility manufactures and sells printed circuit boards (PCBs) or other electronic interconnection products to other companies. What products do you make for sale?				
	One and two-sided rigid, multilayer printed boards	☐ Flexible printed boards	☐ Other interconnections		
	Electronic Manufacturing Se	ervices (EMS) Companies			
	s facility manufactures printed circuit ducts for sale.	assemblies, on a contract basis, a	and may offer other electronic interconnection		
	OEM — Original Equipment	Manufacturers			
	This facility purchases, uses and/or manufactures printed circuit boards, or other interconnection products for use in a final product, which we manufacture and sell.				
١	What is your company's primary prod	uct line?			
_	Industry Suppliers				
This	s facility supplies raw materials, equi	pment or services used in the man	ufacture or assembly of electronic products.		
١	What industry segment do you supply	? PCB EMS Both			
١	What products do you supply?				
	Government, Academic, Non	Profit			
	e are representatives of a government ectly concerned with design, researcl		ical institute or nonprofit organization who are connection devices.		
	Consultant				
١	What services do you provide?				



# **Application for Site Membership**

#### **Site Information**

Company Name			
Street Address			
City	State	Zip/Postal Code	Country
Main Switchboard Phone No.		Main Fax	
Company E-mail address		Web site URL	
Name of Primary Contact			
Title	Mail Stop		
Phone	Fax	E-mail	
Payment Information			
Membership Dues (membership will begin th	ne day we receive your applicat ce indicated below.) All fees qu	· ·	vill continue for one or two
Primary facility:		l <u> </u>	institutions, nonprofit organizations
One year \$1000.00 Two years \$1,800.00	SAVE 10%)	One year \$250.00 Two years \$450.00	SAVE 10%)
already has a different location v  One year \$800.00 Two years \$1,440.00 (\$  Companies with an annual r  One year \$600.00	for a facility of an organization that with a primary facility membership SAVE 10%) revenue of less than \$5,000,000	Consultant (employing less  One year \$600.00 Two years \$1080.00 (	than 6 individuals) SAVE 10%)
Enclosed is our check for S Please bill my credit card:	•	☐ American Express  Expiration Date	□ Visa □ Diners Club
Authorized Signature			
Mail application with class and the second s	vith credit card payment to:	•	ttach business card nary contact here
*Overnight deliveries to this address only.		01/08	



# GET AHEAD ...

# with IPC Training & Certification Programs

Smart decisions and top-notch quality are critical to success — particularly in the highly competitive, ever-changing electronic interconnection industry. Training alone may help with your quality initiatives, but when key employees actually have an industry-recognized certification on industry standards, you can leverage that additional credibility as you pursue new customers and contracts.



Through its international network of licensed and audited training centers, IPC — Association Connecting Electronics Industries® offers globally recognized, industry-traceable training and certification programs on key industry standards. Developed by users, academics and professional trainers, IPC programs reflect a standardized industry consensus. In addition, the programs are current: Periodic recertification is required, and course materials are updated for each document revision with support from the same industry experts who contributed to the standard.

#### Why Pursue Certification?

Investing in IPC training and certification programs can help you:

- · Demonstrate to current and potential customers that your company considers rigorous quality control practices very important.
- Meet the requirements of OEMs and electronics manufacturing companies that expect their suppliers to have these important credentials.
- Gain valuable industry recognition for your company and yourself.
- · Facilitate quality assurance initiatives that have become important in international trading.

#### **Choose From Two Levels of Certification**

Two types of certification are available, each of which is a portable credential granted to the individual in the same manner as a degree from a college or trade school.

**Certified IPC Trainer (CIT)** — Available exclusively through IPC authorized training centers, CIT certification is recommended for individuals in companies, independent consultants and faculty members of education and training institutions. Upon successful completion of this train-the-trainer program, candidates are eligible to deliver CIS training. They also receive materials for conducting application-level (CIS) training.

**Certified IPC Application Specialist (CIS)** — CIS training and certification is recommended for any individual who uses a standard, including operators, inspectors, buyers and management.

#### Earn Credentials on Five Key IPC Standards

Programs focused on understanding and applying criteria, reinforcing discrimination skills and supporting visual acceptance criteria in key standards include:

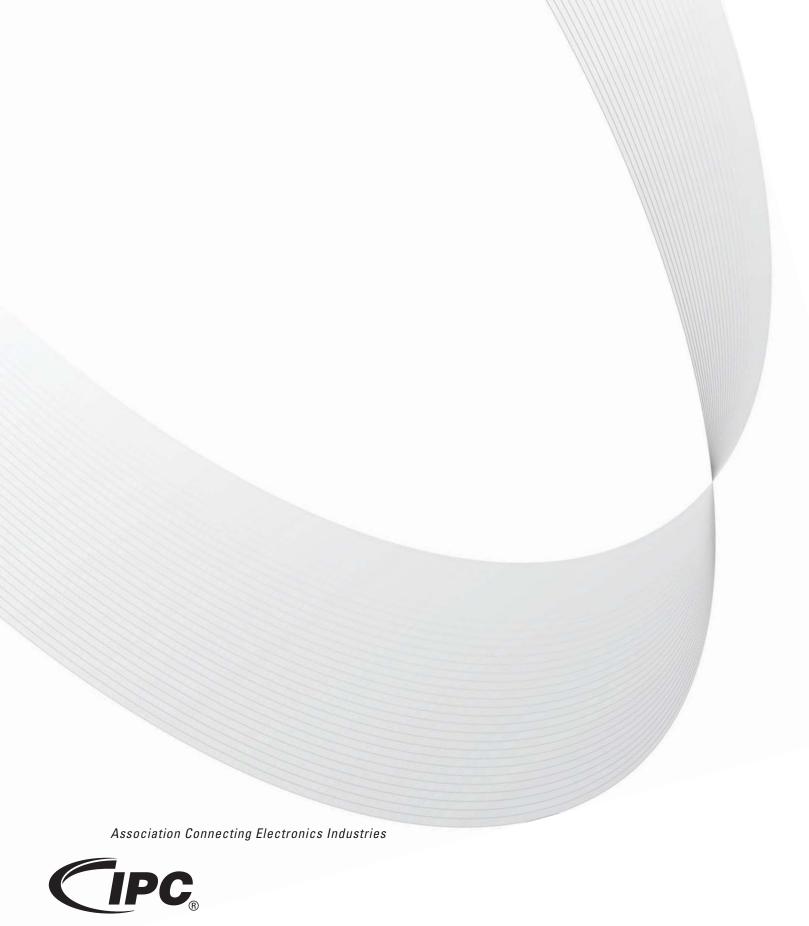
- IPC-A-610, Acceptability of Electronic Assemblies
- IPC-A-600, Acceptability of Printed Boards
- IPC/WHMA-A-620, Requirements and Acceptance for Cable and Wire Harness Assemblies

Programs covering standards knowledge plus development of hands-on skills include:

- J-STD-001, Requirements for Soldered Electrical and Electronic Assemblies
- IPC-7711/IPC-7721, Rework of Electronic Assemblies/Repair and Modification of Printed Boards and Electronic Assemblies

#### Get Started by Contacting Us Today

More than 250,000 individuals at thousands of companies worldwide have earned IPC certification. Now it's your turn! For more information, including detailed course information, schedules and course fees, please visit **www.ipc.org/certification** to find the closest authorized training center.



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847-615-7100 **tel** 847-615-7105 **fax** www.**ipc**.org

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